TM 11-6625-2921-14&P

TECHNICAL MANUAL

OPERATOR'S, ORGANIZATIONAL, DIRECT SUPPORT,
AND GENERAL SUPPORT MAINTENANCE MANUAL
INCLUDING REPAIR PARTS AND SPECIAL TOOLS LISTS
FOR

SIGNAL GENERATOR SG-1054/G
(STELMA MODEL PG-303A)
(NSN 6625-00-137-7738)

HEADQUARTERS, DEPARTMENT OF THE ARMY
16 JANUARY 1980

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Technical Manual

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OPERATOR'S ORGANIZATIONAL, DIRECT SUPPORT, AND GENERAL SUPPORT MAINTENANCE MANUAL INCLUDING REPAIR PARTS AND SPECIAL TOOLS LISTS FOR SIGNAL GENERATOR SG-1054/G (STELMA MODEL PG-303A) (NSN 6625-00-137-7738)

REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mall your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms), or DA Form 2028-1 located in back of this manual direct to: Commander, US Army Communications and Electronics Materiel Readiness Command, ATTN: DRSEL-ME-MQ, Fort Monmouth, New Jersey, 07703.

In either case, a reply will be furnished direct to you.

This manual is an authentication of the manufacturer's commercial literature which, through usage, has been found to cover the data required to operate and maintain this equipment. The manual was not prepared in accordance with military specifications; therefore, the format has not been structured to consider categories of maintenance.

CONTENTS

CONTENTS - Continued

0. INTRODUCTION

(A) Scope

0.01 This manual describes Signal Generator SG-1054/G and provides instructions for operation and maintenance. Throughout this manual, the SG-1054/G is referred to as the Pattern Generator.

(B) Indexes of Publications

0.02 DA Pam 310-4. Refer to the latest issue of DA Pam 310-4 to determine whether there are new editions, changes, or additional publications pertaining to the equipment.

0.03 DA Pam 310-7. Refer to DA Pam 310–7 to determine whether there are modification work orders (MWO's) pertaining to the equipment.

(C) Maintenance Forms, Records, and Reports

0.04 Reports of Maintenance and Unsatisfactory Equipment. Department of the Army forms and procedures used for equipment maintenance will be those prescribed by TM 38-750, The Army Maintenance Management System.

0.05 Report of Packaging and Handling Deficiencies. Fill out and forward DD Form 6 (Packaging Improvement Report) as prescribed in AR 700-58/ NAVSUPINST 4030.29/AFR 71-13/MCO P4030.29A, and DLAR 4145.8.

0.06 Discrepancy in Shipment Report (DISREP) (SF 361). Fill out and forward Discrepancy in Shipment Report (DISREP) (SF 361) as prescribed in AR 55-38/NAVSUPINST 4610.33B/AFR 75-18/MCO P4610.19C and DLAR 4500.15.

(D) Reporting Equipment Improvement Recommendations (EIR)

0.07 If your Signal Generator SG-1054/G needs improvement, let us know. Send us an EIR. You, the user, are the only one who can tell us what you don't like about your equipment. Let us know why you don't like the design. Tell us why a procedure is hard to perform. Put it on an SF 368 (Quality Deficiency Report). Mail it to Commander, US Army Communications and Electronics Materiel Readiness Command, ATTN: DRSEL-ME-MQ, Fort Monmouth, New Jersey 07703. We'll send you a reply.

(E) Administrative Storage

0.08 To prepare the equipment for administrative storage, ascertain its operability and reliability. In addition, use the proper packing materials.

(F) Destruction of Army Electronics Materiel

0.09 Destruction of Army electronics materiel to prevent enemy use shall be in accordance with TM 750-244-2.

1. GENERAL

1.01 This manual describes installation, operation, theory, and maintenance of the PG-303A Pattern Generator. A complete listing of replaceable parts and complete schematic coverage are provided at the end of the manual.

1.02 The Pattern Generator (Fig. 1) is a compact, solid-state digital test set designed to generate a wide variety of telegraph test signal patterns having predetermined and controllable characteristics and parameters. The Pattern Generator is intended for use in conjunction with associated data measuring equipment to test and and evaluate the performance of data/telegraph systems or equipment.

(A) Electrical Description

1.03 The Pattern Generator functions as a self-contained test signal generator operating from a 115/230-volt ac power source. For descriptive purposes the unit may be considered to consist of four principal sections:

(a) Signal patterns and modes.

(b) Distortion generation.

(c) Output circuits.

(d) Power supplies.

Signal Patterns and Modes

1.04 The Pattern Generator is capable of generating the following telegraph code output signal patterns:

(a) Steady Mark or steady Space.

(b) Reversals. Alternate Mark and Space bits in a serial stream at the selected bit rate.

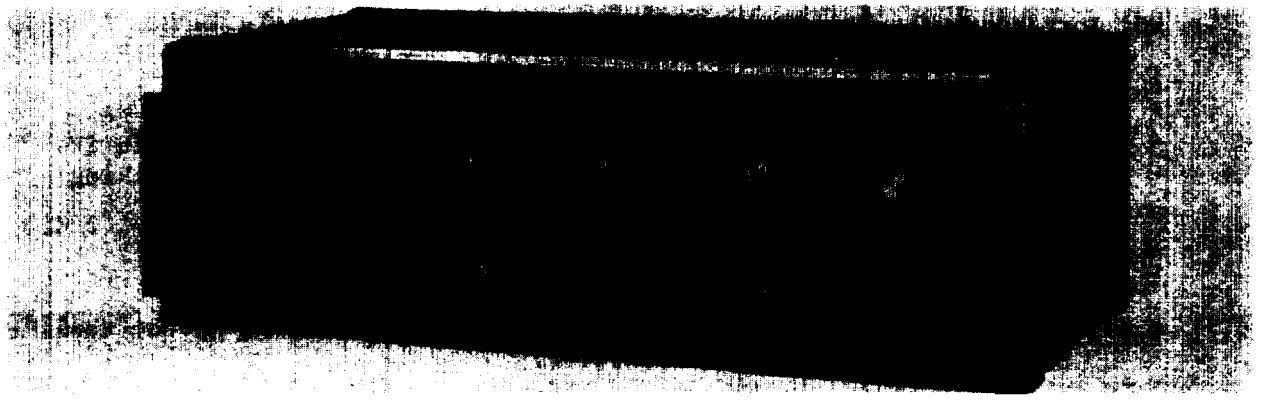


Fig. 1 - Front View - PG-303A Pattern Generator

(c) Selected Characters. A repeating sequence of one to six characters; these characters may be 5-, 6-, 7-, or 8-level code. A carriage-return/line-feed sequence is automatically inserted after each 72 characters in the 5-level and 8-level code. This automatic feature may be disabled via a rear-panel control switch. If less than six characters is generated, the balance of unselected characters will be "filled out" as a steady Mark to allow for answer-back character-receipt or other test purposes.

(d) FOX Message. A 5-level (baudot) or 8-level (ASCII) FOX test message having the following contents:

5-Level (Baudot) Test Message

<< ≡ ↓ THE > QUICK > BROWN > FOX > JUMPS > OVER > THE > LAZY > DOG
> ↑ 1234567890 > ↓ DE >ABCDEF > TEST ↓

8-Level (ASCII) Test Message

DEL << ≡ THE > QUICK >BROWN > FOX > JUMPS > OVER > THE > LAZY > DOG
>1234567890 >DE > DEL DEL >ABCDEF > TEST

Symbol Legend:
< Carriage return
≡ Line feed
> Space
↑ Upper case characters
↓ lower case characters
DEL Delete

Note: The group of six representative characters, ABCDEF, is not a fixed part of the FOX message. This group is derived from the front-panel switch matrix. The operator may program any six station identification characters for this portion of the total test message.

(e) Random Pattern. A repeating 511-bit (common or CCITT) or 2047-bit pseudo-random pattern for making error-count tests.

1.05 The test patterns may be produced as a repetitive serial stream (free running) or may be stepped one character or one sequence at at time by use of a front-panel control or by receipt of an externally generated step pulse.

1.06 The test patterns may be start-stop, with 1-, 1.5- or 2-element stop Marks, or synchronous. The synchronous test patterns do not contain start pulses or stop Marks in the character sequences.

1.07 The test patterns can be generated at any one of 17 bit rates that are switch-selectable from the front panel. Ten of the bit rates are generated by an internal

clock, and one bit rate is derived from an externally generated timing signal. Plug-in crystal sockets are provided for six customer-specified bit rates in conjunction with six optional crystals (see Fig. 2) located on the underside of the unit. All of the bit rates can be selected by a front-panel control.

1.08 The 8-level (ASCII) test patterns may contain a parity-bit in the eighth bit Position. An internal strapping option is provided to permit even, odd, or no parity (Mark always in the eighth bit).

Distortion Generation

1.09 The Pattern Generator output data patterns may be programed with distortion in known, adjustable amounts ranging from 0 to 48 per cent in 1-per-cent increments.

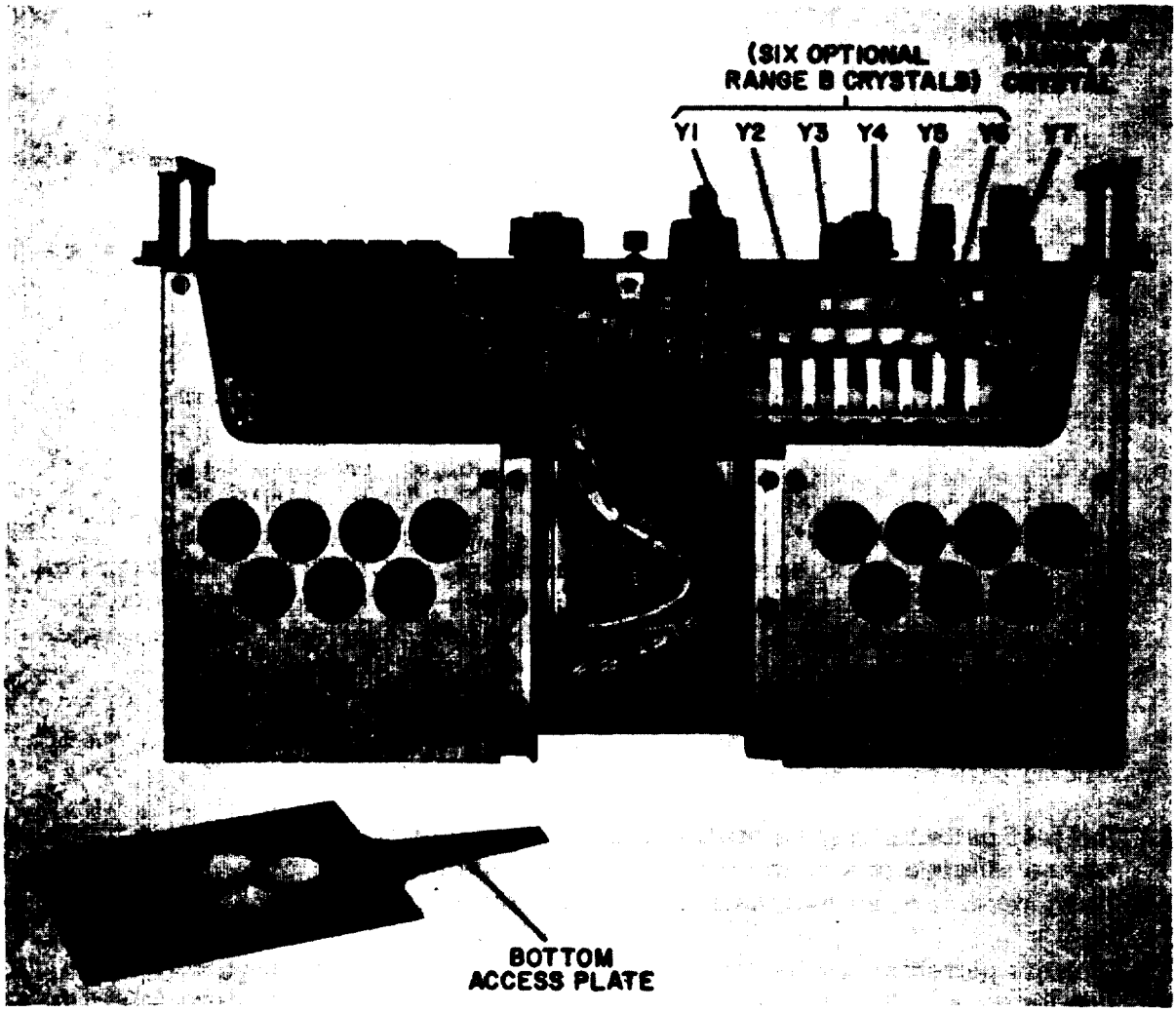


Fig. 2 - Bottom View - Pattern Generator with Access Plate Removed

The type of distortion introduced on the output signal is selectable and may be any one of the following:

(a) Marking bias.

(b) Spacing bias.

(c) Switched bias.

(d) Marking end
(e) Spacing end
} Start-stop signal pattern only.

Output Circuits

1.10 The Pattern Generator output circuits provide two levels of signal output as follows :

(a) Low-level logic (+6 volts) which may be internally strapped to conform with EIA standard RS-232B or MIL-STD-188B.

b) High-level electronic relay contact closures for neutral, polar, or Bell System electronic hub circuits.

1.11 A 12-pin female cable connector for signal interfacing to other data equipment, through an optional Data Set Adapter, is provided on the front panel of the Pattern Generator.

Power Supplies

1.12 Operating power for the Pattern Generator circuitry is derived from three internal, regulated dc power supply circuits furnishing +5 volts, +15 volts, and -15 volts. Fusing protection is provided in the ac primary input circuit and in each dc leg of the three different supply circuits. In addition, an over-voltage protection circuit that protects the integrated-circuit modules from bum-out is an integral part of the +5-volt power supply. Operating ac power is applied via a detachable ac line cord to a connector at the rear of the unit and is controlled by a front-panel illuminating rocker switch.

(B) Equipment Description

1.13 The Pattern Generator may be contained in a portable carrying case, or it may be adapted to rack mounting by using a pair of mounting brackets. The portable carrying case consists of detachable front and rear covers. Storage space is provided in the front cover for the power and signal cables.

1.14 All operating controls and indicators are mounted on the front panel. Fuses and infrequently used connectors and terminals are located on a small sub-panel having a hinged door at the rear of the unit (see Fig. 3). Access to the eight plug-in printed-circuit (PC) cards is obtained at the rear of the unit. It is not necessary to

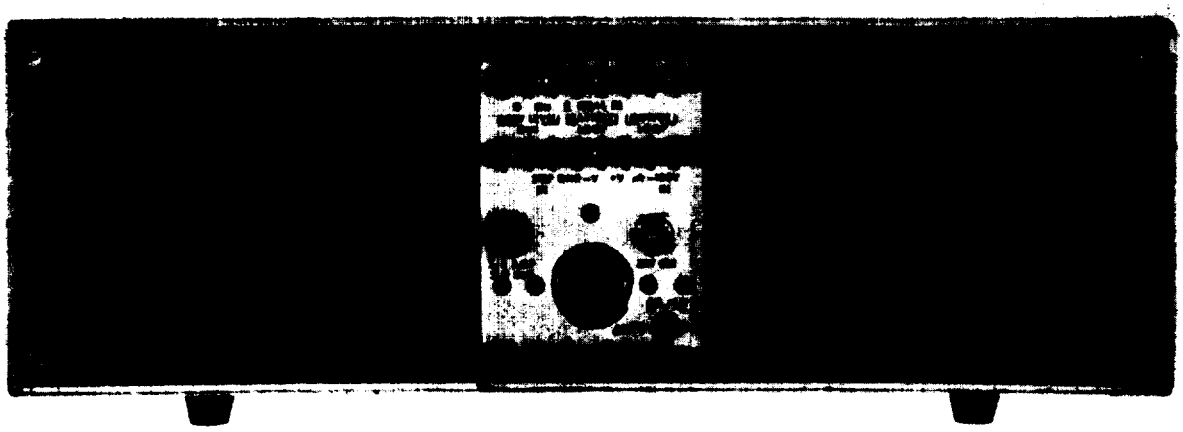


Fig. 3 - Rear View - Pattern Generator with Panel in Place

remove the chassis from the metal cabinet in order to remove these assemblies. A PC-card extender for test and troubleshooting is provided and stored in the slot marked A9, directly under assembly A7 (see Fig. 4).

(C) Performance Specifications

1.15 Performance specifications for the Pattern Generator are provided in Table I, which includes a description for each performance item listed.

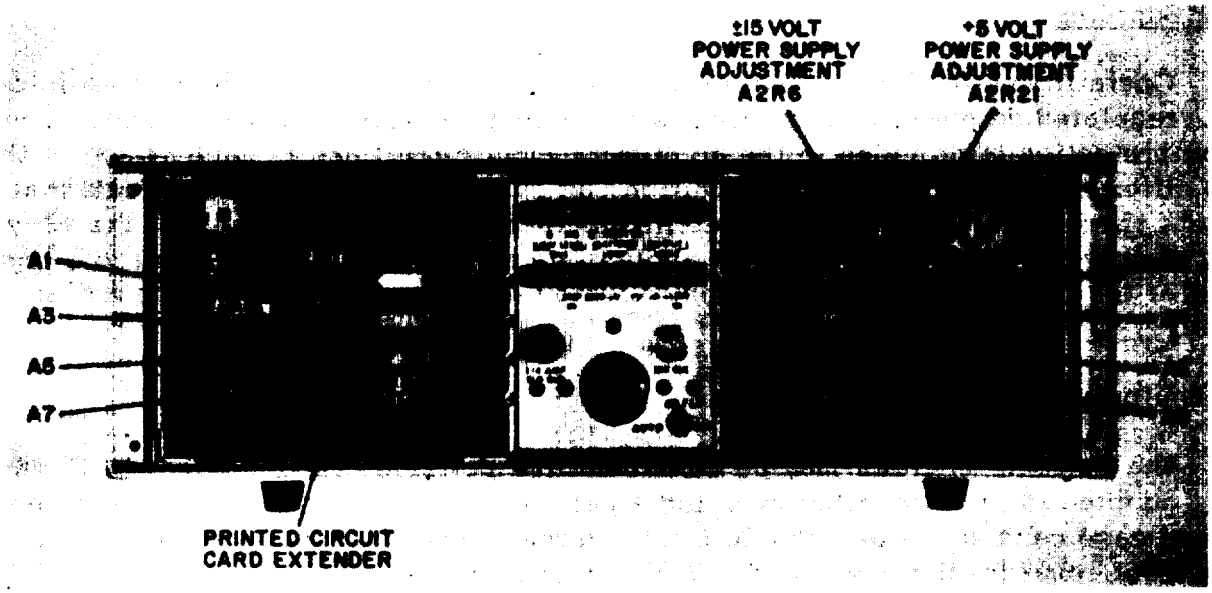


Fig. 4 Rear View- Pattern Generator with Panel Removed

TABLE I

PERFORMANCE SPECIFICATIONS

ITEM	DESCRIPTION
Output Signals:	
Patterns	FOX message (S-level or 8-level code), reversal! selected characters (5-, 6-, 7-, 8-level code), random pattern and steady Mark or Space.
Bit Rates	Ten fixed rates (bits per second): 37.5, 50, 75, 150, 300, 600, 1200, 2400, 4800, 9600. Input for external timing source, and provisions for six plug-in crystals providing six additional rates (customer option).
External Timing Signal Requirements	Polar square-wave, ±6 volts, at 200 times the desired data rate.
Programmable Distortion:	
Types	Marking bias, Spacing bias, switched bias (alternate Mark/Space bias on a character basis) Marking end, and Spacing end.
Amount	0 to 48 per cent in 1-per cent steps.
Modes:	
Synchronous:	Free-run and external bit sync.
start-stop:	Free-run and stepped (manually or externally)
output Levels:	
High	Polar, +130 to -130 volts, 10 to 30ma; neutral, zero to 230 volts, 20 or 60ma; Bell System electronic hub, -130-volt Space closure to standard hub pot. (Loop batteries externally supplied.)
Low	Low-level logic output (±6 volts) in accordance with MIL-STD-188B or EIA standard RS-232B.

TABLE I (Cont'd)

ITEM	DESCRIPTION
External Character-Stepping Signal Requirements:	Polar (±6-volt) square -wave, or positive pulse 0 to +6 volts.
Power Requirements	115/230 volts +10%, 50 to 400Hz ±5%, 20 watts.
Dimensions	17 1/2 inches wide by 5 13/16 inches high by 12 1/4 inches deep.
Weight	18 pounds (approximately) in carrying case.

(D) Description of Controls and Indicators

1.16 Fig. 5 shows all controls and indicators used during normal operation of the Pattern Generator, and Table II lists and identifies the reference designation and function of each control and indicator. The rear-panel terminals and controls are listed and described in Table III and illustrated in Fig. 3.

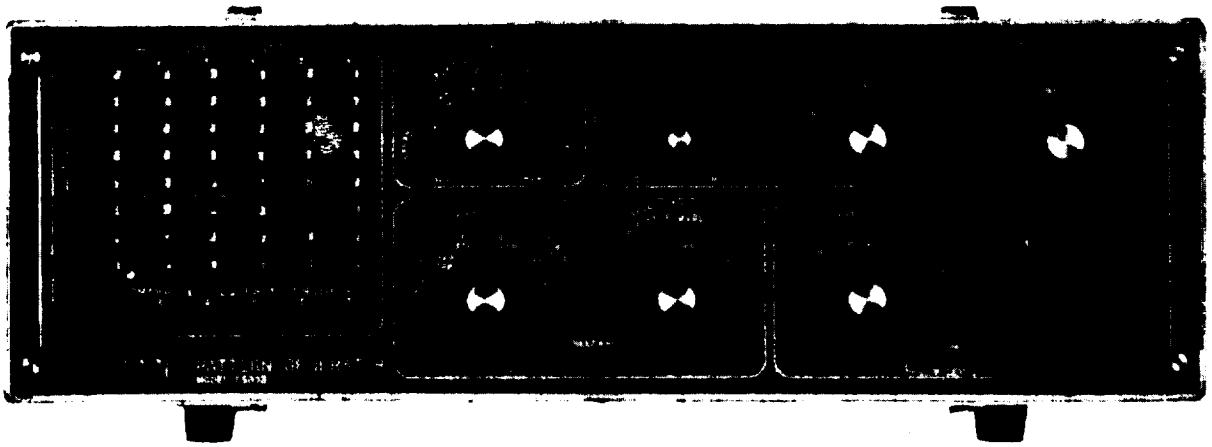


Fig. 5 - Front Panel Controls - Pattern Generator

TABLE II

CONTROLS AND INDICATORS

NAME AND TYPE	REF DES	CONTROL POSITION	FUNCTION
SELECTED CHARACTERS (48 red pushbutton switches)	S10A through S10H, S15A through S15H	Characters 1 through 6 (8 bits per character)	Provide means for programing the six selected characters of output test signal. When a given switch is depressed, the bit for that position becomes a Mark. Undepressed switches produce Spaces.
CHARACTER SEQUENCE LENGTH (6 black pushbutton switches)	S16A through S16F	(Characters 1 through 6)	Each numbered switch, when depressed, establishes length of the SELECTED CHARACTERS sequence to be generated.
PATTERN selector switch	S2	REV	Causes reversal pattern to be generated (alternate Mark and Space).
		STEADY:	
		M	Causes a continuous Mark output signal to be generated.
		S	Causes a continuous Space output signal to be generated.
		SELECTED CHARACTERS - CODE LEVEL: 5, 6, 7, and 8	Establishes 5-, 6-, 7-, or 8-level code format for characters preset by SELECTED CHARACTERS pushbutton switches.
		FOX MSG: 5, and 8	Selects programed FOX message to be generated in 5-level code (baudot) or 8-level code (ASCII).
		RAND	Selects random bit pattern (internally strapped for 511-bit or 2047-bit format) to be generated.

TABLE II (Cont 'd)

NAME AND TYPE	REF DES	CONTROL POSITION	FUNCTION
DISTORTION switches:			
PERCENT (dual-concentric switches)	S5	0 through 40 (inner knob, red markings)	Selects increment of distortion, in steps of 10%, up to 40%. Add to 1% settings below to produce total distortion generated.
		0 through 9 (outer knob, black markings)	Selects increments of distortion, in steps of 1%, up to 9%. Added to 10% (incremental) setting above to produce total distortion generated.
TYPE	S7	OFF	In this position, no distortion is introduced on signal output.
		BIAS:	
		M	Selects Marking bias distortion.
		S	Selects Spacing bias distortion.
		SW	Selects switched bias distortion (on a character basis).
		END:	
		M (applicable to start-stop mode only)	Selects Marking end distortion.
		(applicable to start-stop mode only)	Selects Spacing end distortion.

TABLE II (Cont 'd)

NAME AND TYPE	REF DES	CONTROL POSITION	FUNCTION
BIT RATE dual-concentric switch	S1 411S1)	A/B range selector (inner knob, red markings).	Selects upper (A) or lower (B) scales of bit-rate dial.
		Frequency selector (outer knob)	Selects rate of data output signal (in bits per second).
MODE switches:			
(left switch)	3	FREE RUN	Selected output signal pattern is generated repetitively at selected internal bit rate.
		EXTERNAL:	External step signal is applied to rear-panel STEP IN connector.
		CHAR. STEP (applicable to start-stop mode only)	Each character of the selected signal pattern is generated (stepped) by each externally applied step pulse signal.
		SEQ STEP (applicable to start-stop mode only)	One complete selected pattern sequence is generated (once) by each externally applied step signal.
		BIT SYNC (applicable to synchronous mode only)	Pattern Generator operates at the externally applied bit timing signal rate. Distortion cannot be introduced on the output pattern.
		MAN STEP:	
		CHAR (applicable to start-stop mode only)	In conjunction with associated RELEASE pushbutton switch, causes one character at a time to be generated with each actuation

TABLE II (Cont' d)

NAME AND TYPE	REF DES	CONTROL POSITION	FUNCTION
		SEQ (applicable to start-stop mode only)	In conjunction with associated RELEASE pushbutton switch, causes one entire character pattern sequence to be generated with each actuation of the RELEASE pushbutton.
RELEASE push-button switch	S4	- - - - - - -	Provides for manual stepping of output characters and sequences.
(Right switch)	S6	S TART/S TOP UNIT STOP MARK:	
		1.0	Stop-Mark duration = 1.0 bit unit.
		1.5	Stop-Mark duration = 1.5 bit units.
		2.0	Stop-Mark duration = 2.0 bit units.
		SYNC	Output data is generated in synchronous form (a continuous data stream without start-Spaces and stop-Marks).
OUTPUTS (switch, indicator, and connectors):			
HI-LEVEL SELECT switch	S9	NEUT	Sets conditions for keying neutral loop signal (up to 230 volts at 60ma, max) at HI-LEVEL output phone jack and rear-panel terminals. (Battery and loop resistor externally supplied.)

TABLE II (Cont'd)

NAME AND TYPE	REF DES	CONTROL POSITION	FUNCTION
		POLAR	Sets conditions for keying polar loop (±130 volts at 20 to 30ma) at HI-LEVEL output phone jack and rear-panel terminals. (Battery and loop resistor externally supplied.)
		HUB	Sets conditions keying a HUB circuit (+60-volt Mark to - 30 - volt Space) at HI-LEVEL output phone jack and rear-panel terminals. (Battery externally supplied.)
SIG indicator lamp, clear	DS1	------	Lights when a Mark is being generated.
LOW LEVEL output terminals:			
SIG	TP1	SIG	Low-level (±6 volts) output signal terminal.
GND	TP2	GND	Low-level output signal ground terminal.
HI-LEVEL phone jack	J1	------	Provides signal output connection for high-level (loop) output signals.
Unmarked 12-pin cable connector	J2	------	Provides signal output connections for interfacing via Data Set Adapter to other equipment.
POWER/OFF illuminated rocker switch	S8	------	Controls application of ac line power to unit,

TABLE III

REAR-PANEL CONTROLS AND TERMINALS

NAME AND TYPE	REF DES	CONTROL POSITION	FUNCTION
(Two 7-terminal barrier strips)	A12TB1, A12TB2	- - - - -	Provides duplicate connections for front -panel, low-level out - put terminals and high-level output jack. Also provides for connection of external loop batteries and external stepping signal input.
1/4 AMP SLO BLO fuse	A12F1	- - - - -	AC power line fuse. (DC power supply fuses located internally on Assembly A2.)
EXT CLK coaxial connector	A12J2	- - - - -	BNC-type connector for apply- ing external bit-rate timing signal.
Unmarked re - cessed male cable connector	A12J1	- - - - -	Twist-lock connector for de- tachable ac power cord.
CR/LF switch	A12S1	AUTO	Sets conditions for automatic generation of a carriage-return and line-feed signal after 72 characters in 5-level and 8- level modes.
	(A12S1)	OUT	Disables automatic generation of carriage-return and line- feed signal.

(E) Installation

Physical and Mechanical Considerations

1.17 The Pattern Generator may be installed and used in two different ways:

(a) As a piece of portable test equipment enclosed in an optional carrying case utilizing a removable cover having cable storage provisions.

(b) In a semi-premanent rack or cabinet installation wherein the unit is mounted and wired in a way that precludes frequent changes of location.

1.18 The over-all dimensions of the basic unit are shown in Fig. 6 along with the dimensions of the carrying case for portable use. When used in standard 19-inch rack -mount installations, the required 19-inch width is obtained by two brackets which fasten to the sides of the unit. In the portable configuration, the Pattern Generator will normally be carried to the point of use and set up on a bench or table. Since this type of installation will usually be temporary, the usual handling practices and precautions taken with quality portable test equipment in field use will generally suffice.

1.19 When the Pattern Generator is to be rack- or cabinet-mounted, the unit should be installed at a working height that enables convenient access to panel controls and markings. Avoid locating the unit above or near equipments generating large amounts of heat. Consideration should also be made in planning the location and routing of connecting wiring and cables to prevent undesirable interaction with other equipment.

Electrical Connections

1.20 Installation or application of the Pattern Generator in a given situation will require wiring connections to be made to and from the terminals and connectors on the front and rear panels of the unit. In addition, a particular application may require that certain internal wiring (strapping) connections be made or changed. Several of the printed-circuit assemblies of this unit contain strapping terminals for these alternate circuit configurations to satisfy the requirements of different system applications and uses. For instance, the selection of odd or even parity-bit generation (or no parity-bit) is made by a strapping connection on PC-card A8. Instructions for these various strapping options are given in 1.24 below.

External Wiring Connections

1.21 The output terminals for both the high-level and low-level signals located on the front panel are duplicated at a terminal board on the rear panel of the unit. Choice of which output terminals to use in a given situation will be governed by the individual circumstances of each installation or use. When the pattern Generator is used in high-level telegraph circuits, the required loop battery connections are made at the rear-panel terminal boards. External timing signals and external character stepping signals, when used, are also applied via rear-panel connections.

1.22 Wiring connections for hub operation and the various modes of high-level loop operation are shown in Fig. 7 through 13. Polarities shown should be carefully observed. The Pattern Generator provides only dry-contact closures for the high-level output circuits: therefore, the user of this equipment must ensure that adequate current-limiting resistance is present in the external loop circuit. For this reason, a representative variable resistance symbol is shown connected in series with the loop supply in these illustrations. The resistance value will be determined by the individual loop requirements and, thus, no specific ohmic values are given.

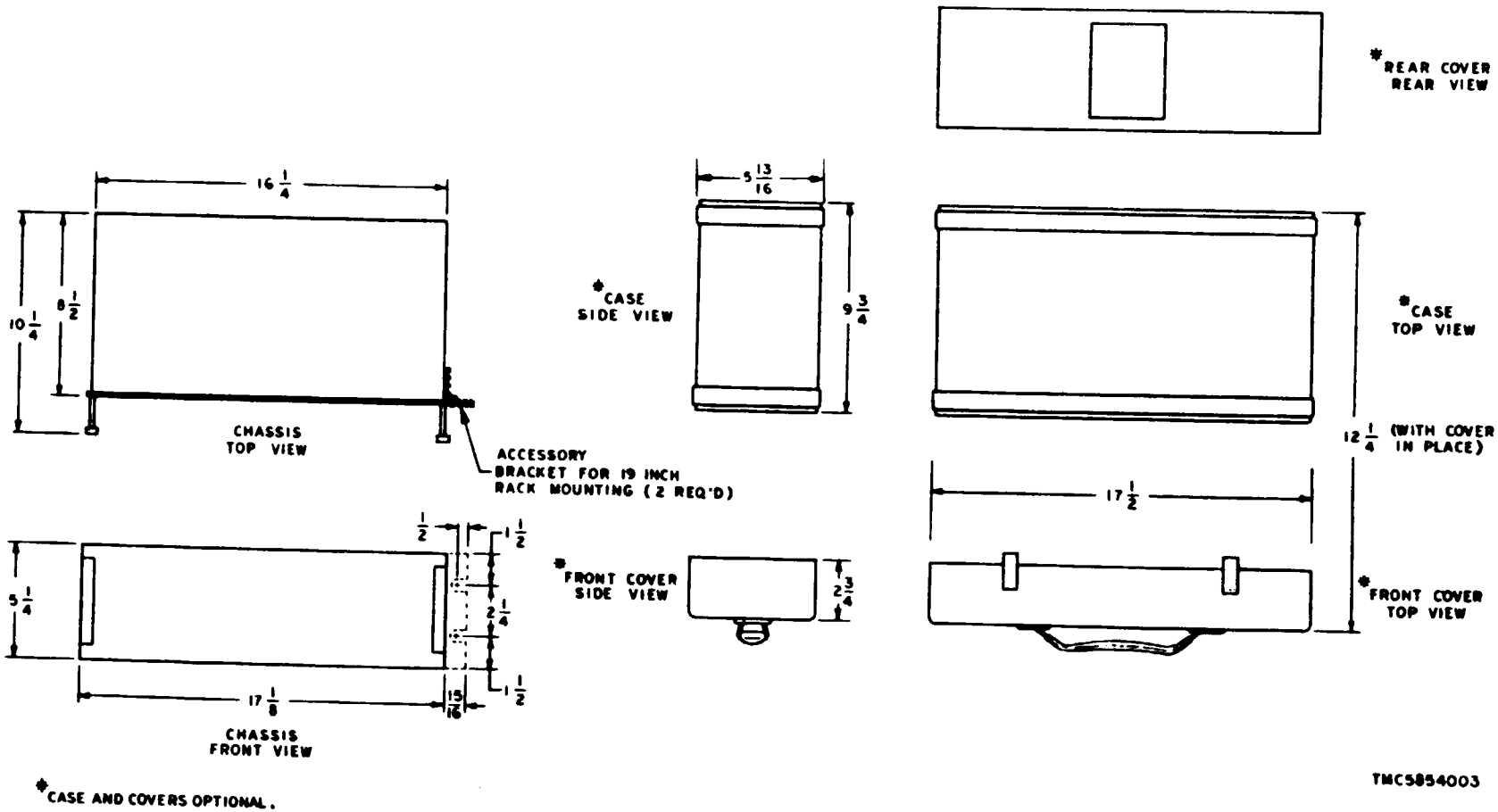


Fig. 6 - Outline Drawing - Pattern Generator

1.23 The high-level output circuits of the Pattern Generator contain full-wave bridge diode configurations which minimize the danger of damage or destruction of Pattern Generator circuit components beta use of incorrect polarity connection of external loop supplies. However, the polarity of the output signal (positive Mark or negative Mark) is affected by the polarity of the loop battery connection. The polarity symbols in Fig. 7 through 13 indicate the relative polarity of the output signal for the various loop battery connections. Reversing the battery polarity will reverse the relative polarities of the Space and Mark output signals.

Internal Strapping Options

1.24 The following Pattern Generator PC-cards contain strapping terminals:

(a) PC -card A1 -- Time-base and oscillator circuits.

(b) PC-card A3 -- Data output circuits.

(c) PC-card A4 -- Message control circuits.

(d) PC-card A7 -- Character distributor and timing control.

(e) PC-card A8 -- Signal pattern matrix.

1.25 Instructions for making strapping connections are given in the next five para - graphs in the same order as listed above. The location of the numbered wiring terminals on each card is illustrated in Fig. 14.

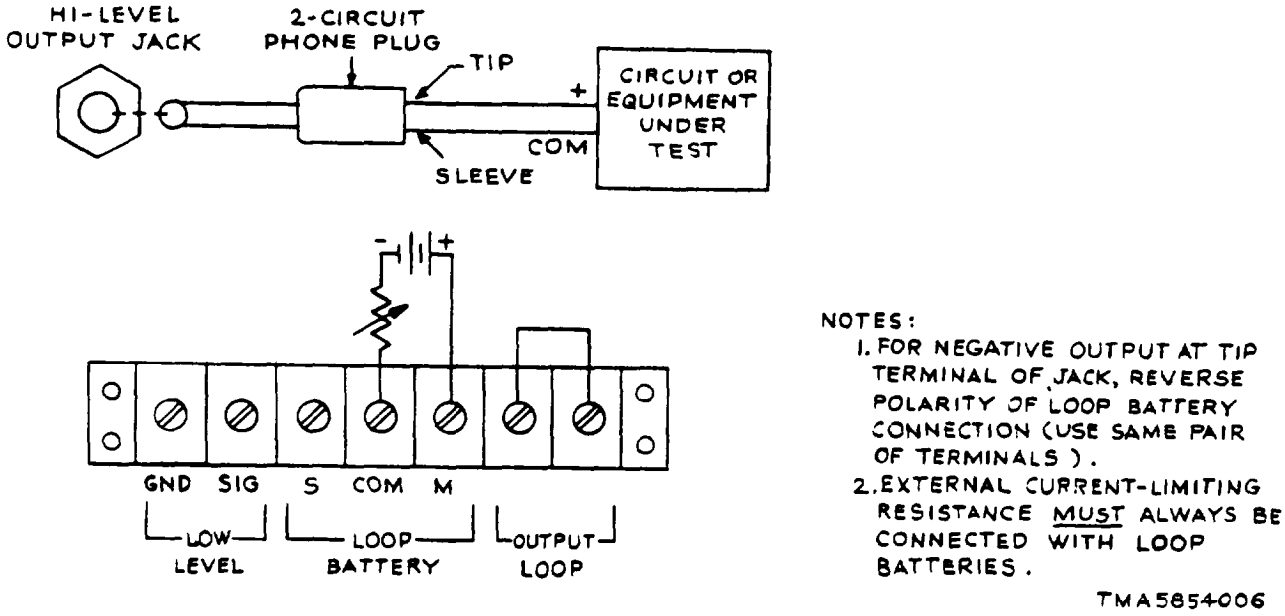


Fig. 7 - High-Level Neutral Operation, Positive Tip, Using Front-Panel Phone Jack for Connection to Loop or Equipment

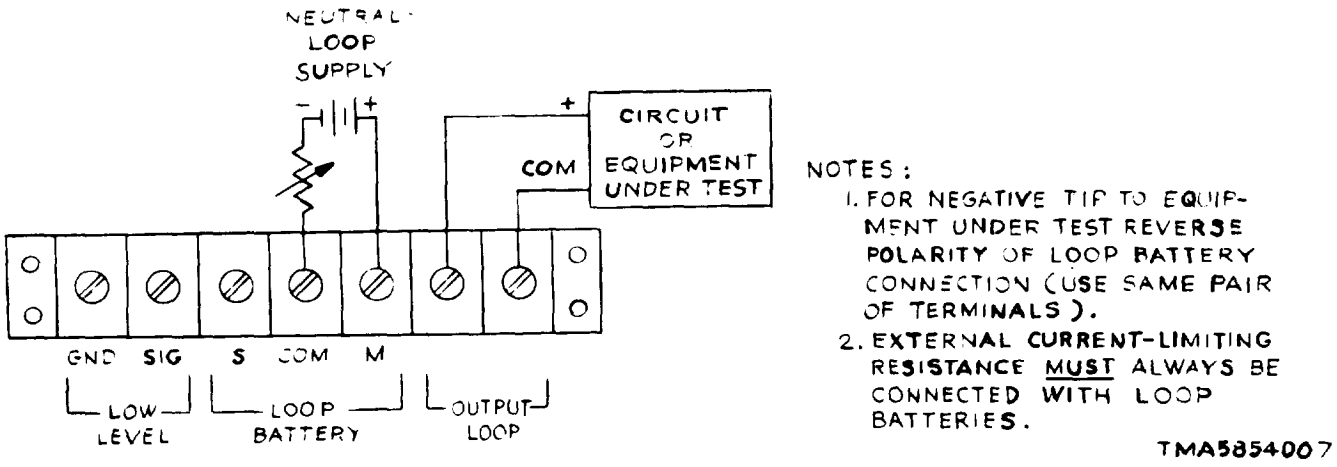


Fig. 8 - High-Level Neutral Operation, Positive Tip, Using Rear-Panel Terminals for Connection to Loop or Equipment

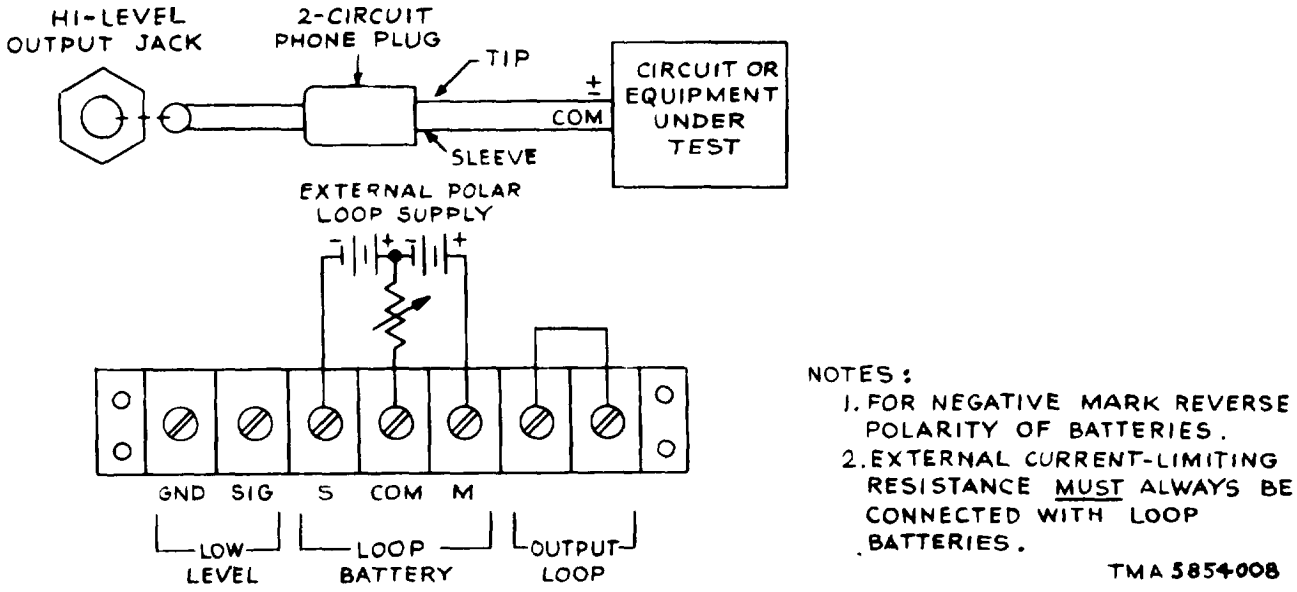


Fig. 9 - High-Level Polar Operation (Positive-Mark), Using Front-Panel Phone Jack for Connection to Loop or Equipment

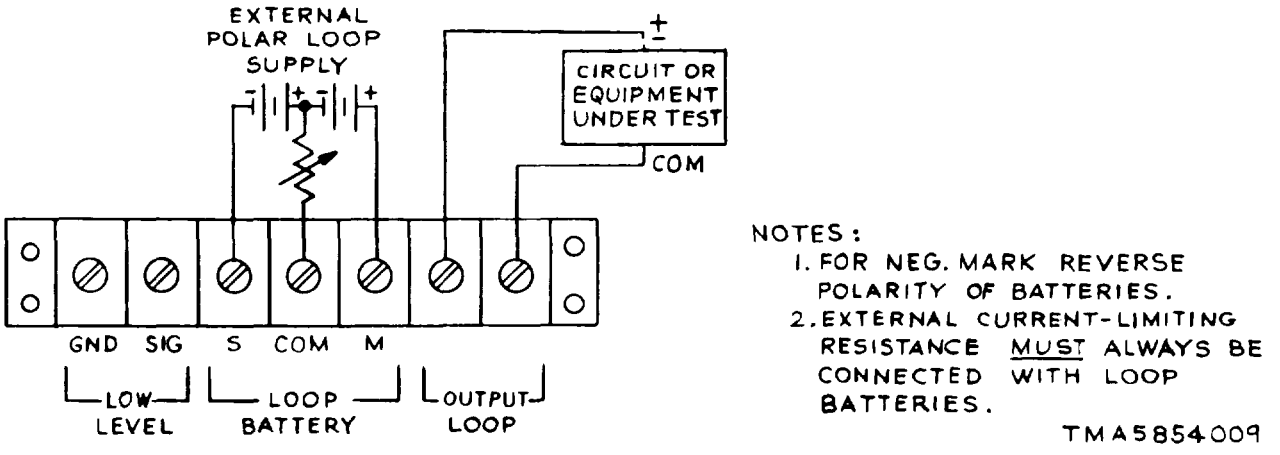


Fig. 10 - High-Level Polar Operation (Positive-Mark), Using Rear-Panel Terminals for Connection to Loop or Equipment

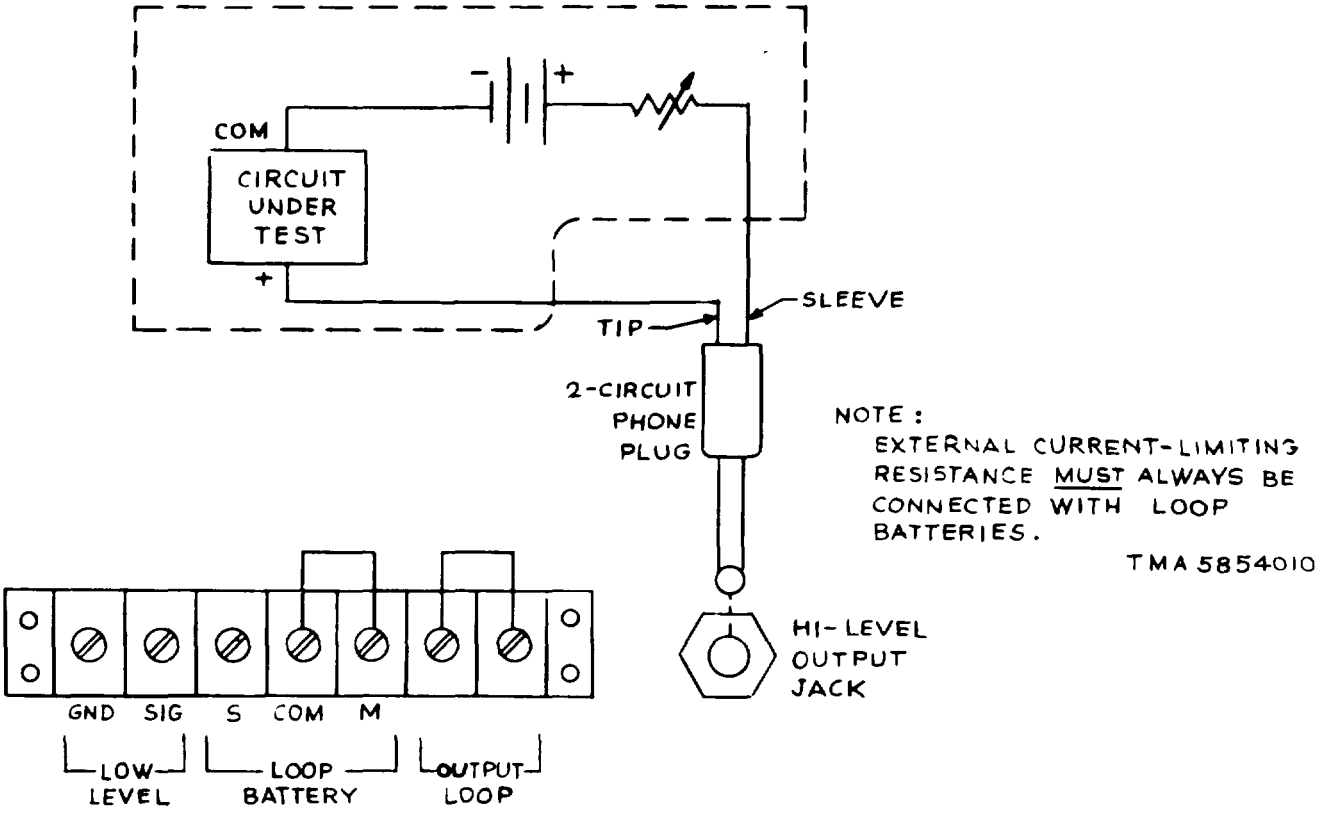


Fig. 11 - Front-Panel Loop Connection, Neutral Operation, for Loop Supply Integral with External Circuit

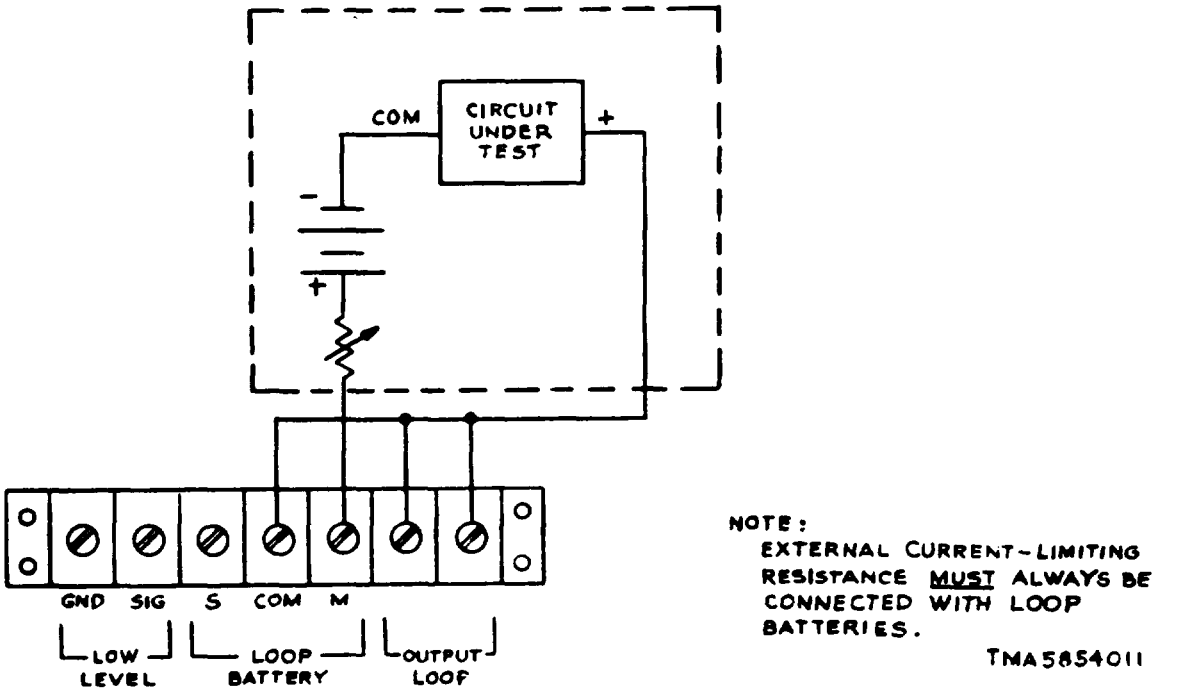


Fig. 12 - Rear-Panel Loop Connection, Neutral Operation, for Loop Supply Integral with External Circuit

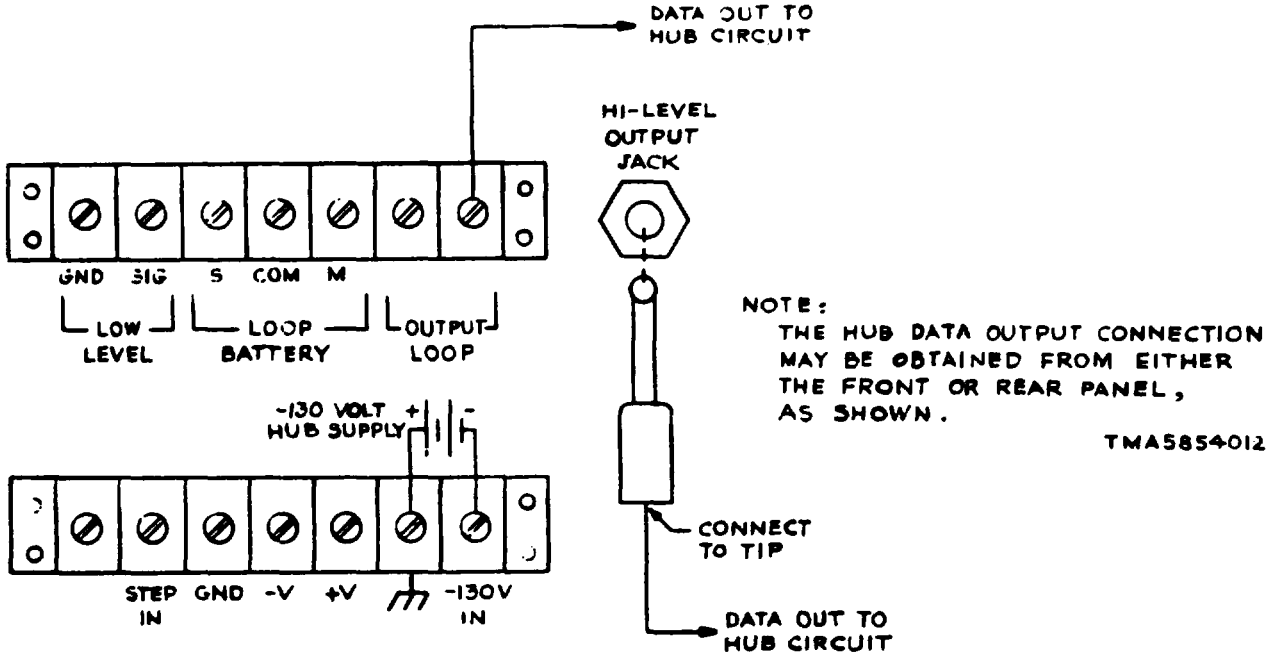


Fig. 13 - External Connections, Hub Operation

(a) The strapping on PC-card A1, Time- Base and Oscillator Circuits, affects the bit-rate selections of the B range of the dual-range time base. The strapping connections provide a choice of three frequency division rates (32, 16, and 1) for the six B-range crystals (see Fig. 2). Each of the six crystals may be connected for any one of the division factors of 32, 16, or 1. In selecting crystals to obtain specific bit rates, the desired bit rate must be multipled by 200 times 32, 16, or 1 to arrive at the crystal frequency. (The output frequency of the time-base circuit is 200 times the bit rate.) The strapping is as follows:

CRYSTAL	DIVISION RATES	STRAPPING CONNECTION:
Y1	32	4 t o 3
	16	4 t o 2
	1	4 t o 1
Y2	32	A t o 3
	16	A t o 2
	1	A t o 1
Y3	32	B t o 7
	16	B t o 6
	1	B t o 5

CRYSTAL	DIVISION RATES	STRAPPING CONNECTIONS
Y4	32	8 t o 7
	16	8 t o 6
	1	8 t o 5
Y5	32	12 to 11
	16	12 to 10
	1	12 to 9
Y6	32	C t o 1 1
	16	C to 10
	1	C t o 9

(b) The strapping on PC-card A3, Data Output Circuits, establishes the Mark polarity of the low-level output signal. Make strap connections as follows:

LOW-LEVEL MARK POLARITY	CONNECTION REQUIRED
Positive (+6 volts)	strap 2 to 5
Negative (-6 volts)	strap 1 to 5

Note: Terminals 1, 2, 3, and 4 for high-level polarity are pre-strapped at the factory as follows: 1 to 4 and 2 to 3. These connections do not require changing. Polarity changes for the high-level output signals may be accomplished by reversing the loop battery connections.

(c) Stropping on PC-card A4, Message Control Circuits, establishes the triggering polarity of the external character-stepping signal and adjusts the input circuit to accommodate a hi-polar (±6 volt) or single-ended positive (0 to +6 volts) stepping signal.

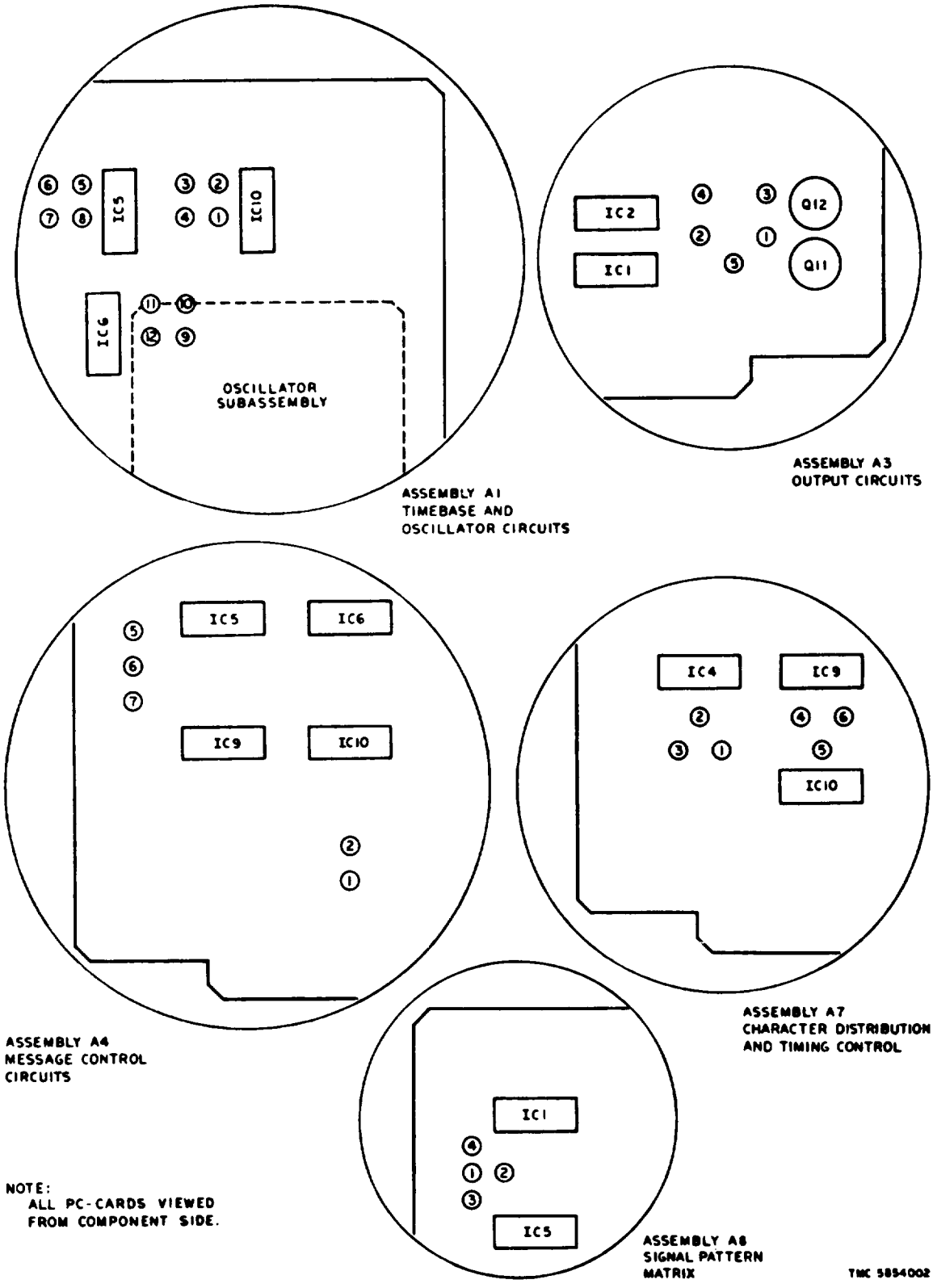


Fig. 14 - PC-Card Strapping Terminal Locations

FUNCTION CONTROLLED	STEPPING SIGNAL CHARACTERISTICS	CONNECTIONS REQUIRED
Triggering Polarity	Positive-going transition	Strap 5 to 6
	Negative-going transition	Strap 7 to 6
Signal Type	Bi-polar (±6-volts; 0-volt threshold)	Strap 1 to 2
	Single-ended positive (0 to +6 volts; 0.7-volt threshold)	No strap (open circuit between 1 and 2)

(d) Strapping on PC-card A7, Character Distributor and Timing Control, establishes the conditions for generation of any of three random pattern signals: a 511 bit common pattern, a 511 bit CCITT standard pattern, and a 2047-bit pattern (RAND setting of PATTERN switch). Make strap connections as follows:

RANDOM BIT PATTERN	CONNECTIONS REQUIRED
511 bit Common Pattern	1-2 and 5-6
511 bit CITT Pattern	2-3 and 5-6

RANDOM BIT PATTERN	CONNECTIONS REQUIRED
2047-bit	1-2 and 4-5

(e) PC-Card A8, Signal Pattern Matrix. The strapping on this PC-card establishes the mode of parity-bit generation when the Pattern Generator is generating the 8-bit ASCII code. The three “choices available are odd parity, even parity, or no parity bit. In the latter case, the bit position will always contain a Mark. Make strap connections as follows:

PARITY MODE	CONNECTION REQUIRED
Odd	Strap 1 to 3
Even	Strap 1 to 4
None	Strap 1 to 2

Power Connections

1.26 The ac power cord of the Pattern Generator is a detachable item that is stored in the hinged cover of the portable unit during storage or while the unit is in transit. The only power connection required in setting up the Pattern Generator for use is the attachment of this ac power cord to the rear-panel connector on the unit and to the ac power source outlet. Connection of external loop batteries is covered in 1.20 through 1.23. Before making power connections for the first time, the input strapping connections should be checked, and changed if necessary, to match the source power at the point of use. The strapping connections provide for wiring the primary input circuit for a 115-volt or 230-volt ac power source. The strapping terminals are accessed by removing the bottom access plate (see Fig. 2). The four numbered terminals are strapped as follows:

INPUT VOLTAGE	STRAP CONNECTIONS
115 volts	Strap terminal 1 to 3
	Strap terminal 2 to 4
230 volts	Strap terminal 2 to 3

Initial Adjustments

1.27 The Pattern Generator requires no adjustments at the time of installation to effect normal operation. The only adjustments in the unit are the power supply voltage adjustments on PC-card A2; these are factory-adjusted and should not require readjustment unless component repairs and replacements have been made in the power supply circuitry. Procedures for power supply adjustments are contained in Maintenance Section 4 of this manual.

2. OPERATION

(A) Circuit Connections

2.01 Connections between the Pattern Generator and the equipment or system under test will generally vary from one application to another. No one fixed procedure or setup will apply to all cases . The Pattern Generator contains the built-in flexibility to accommodate a relatively wide range of functional applications; this variety variety is made available via the provisions for external input and control signals as well as the internal strapping options. The details for making the required connections and strapping are described in the previous section of this manual under (E) Installation.

Generally, the procedure for making circuit connections prior to operating the equipment in a given situation will be as follows:

(a) Determine the mode of operation to be used. Principally, is the output signal to be high-level or low-level?

(b) Determine whether or not any of the internal strapping options require changing.

(c) Determine whether or not any external stepping sources or bit timing signals are to be used (see Table II MODE switches, EXTERNAL). The external step signal is applied to rear-panel STEP IN connector.

(d) When (a) through. (c) above are established, make the applicable connections following the procedures and precautions described under (E) Installation in the first section of this manual.

(B) Operating Procedures

2.02 Before operating the Pattern Generator, make certain that required connections (ac power, loop, signal, etc.) have been properly made for the given application. Refer to 2.01 for explanatory details. After connections are made, turn on the equipment and use the procedures outlined below as a guide in operating the Pattern Generator.

Manipulation of Controls

2.03 Manipulate the Pattern Generator controls as follows:

(a) Select the output bit-rate by setting the appropriate combination of the dual BIT RATE switches. Use the small, inner knob to select range A or B, then use the large, outer knob to select the desired bit-rate.

(b) Select the desired output data pattern by positioning the PATTERN selector switch. If one of the SELECTED CHARACTERS positions or one of the FOX MSG positions is chosen, then the field of SELECTED CHARACTERS switches to the left of the PATTERN switch must be programed as described in (c) below. For all other positions of the PATTERN switch the settings of the SELECTED CHARACTERS push-button switches do not matter.

(c) If a selected character pattern or a FOX message is to be generated, program the applicable bit positions of each vertical group of switches representing the six programmable characters. The 6- character station identification code, which is part of the complete FOX message, is programed by these switches. See Fig. 15 and 16

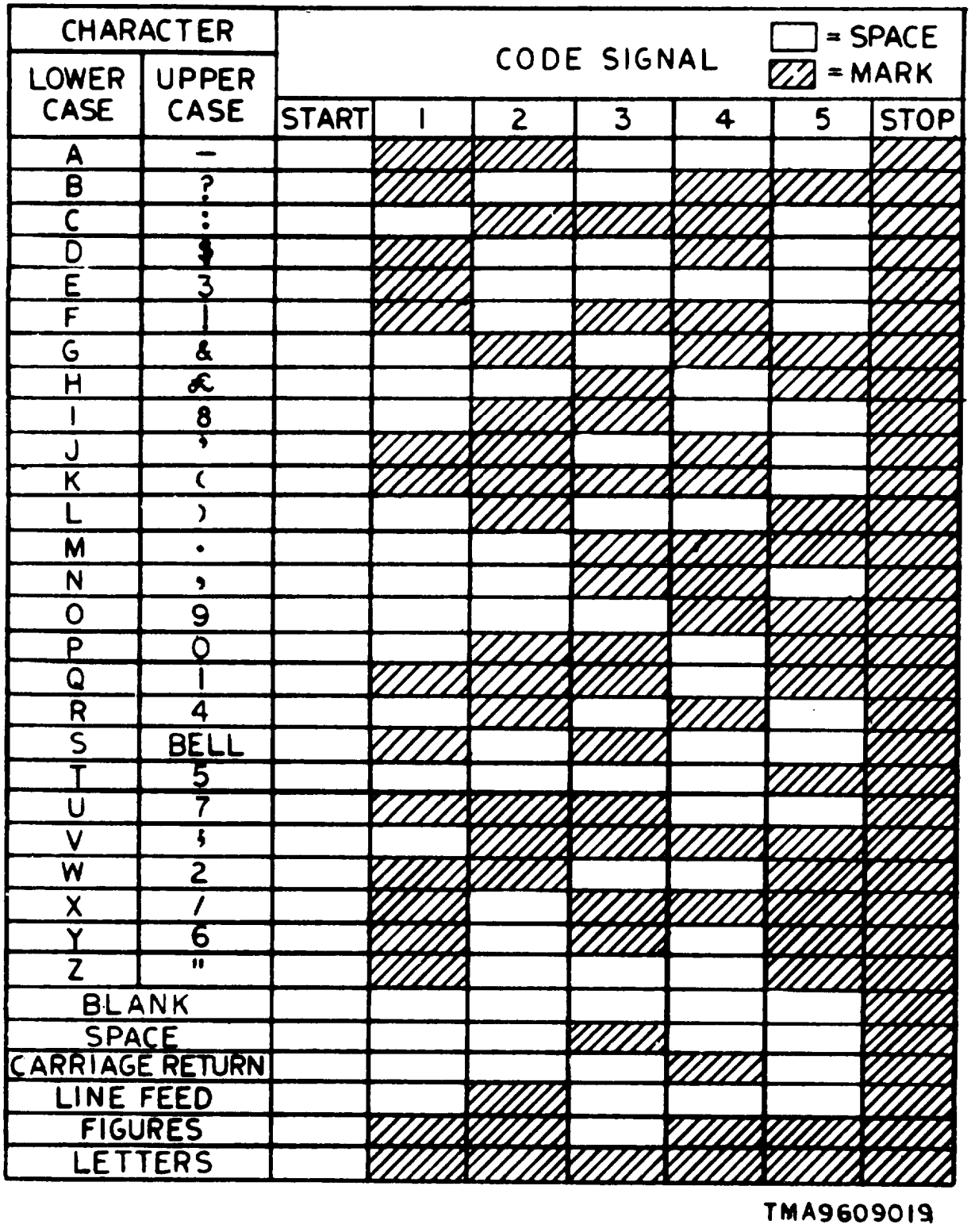


Fig. 15 - Standard 5-Unit Start-Stop Teletypewriter Code

for details of the Mark/Space patterns for both the Baudot and ASCII codes. To program a Mark, the applicable pushbutton should be depressed. Spaces will be generated for those positions where the pushbuttons are not depressed.

(d) Set the rear-panel CR/LF switch to AUTO or OUT to enable or inhibit the automatic generation of a carriage-return, line-feed sequence after generation of 72 characters (applicable to either 5-level or 8-level selected character codes only).

(e) Select the length of the character sequence to be generated by depressing one of the six CHARACTER SEQUENCE LENGTH pushbutton switches. Generally, the stitch selected will be the same as the number of programed characters in the field above, but any number may be selected. (For example, if six characters have been programed and CHARACTER SEQUENCE LENGTH switch number 3 is depressed, only the first three of the s lx selected characters will be generated. A steady Mark will occupy the remaining character intervals.) These switches are functional only for the selected character's positions of the PATTERN switch; they do not affect the FOX message station identification code.

(f) Select the mode of character stepping by setting the left-hand MODE switch to the desired position. In all positions except FREE RUN an external character stepping source is required (see Table II MODE switches, EXTERNAL) . The external step signal is applied to rear-panel STEP IN connector. In the two MAN STEP positions this external stepping is obtained manually by depressing the RELEASE pushbutton switch. In FREE RUN the unit repeatedly generates the selected output pattern without external triggering.

(g) Select the start-stop or-synchronous modes of code transmission by setting the right-hand MODE switch to SYNC or to one of the three START/STOP settings, as required. These latter three settings establish the length (duration) of the stop-Mark bit.

(h) If distortion is to be introduced on the output signal, set the DISTORTION TYPE switch to select bias or end distortion. For zero distortion set this switch to OFF. Select the amount of distortion by operating the dual-concentric PERCENT control. The small, inner knob sets the amount in increments of ten. The larger, outer knob sets the amount in unit increments. The two controls are additive; i.e. , to obtain 15 per cent use settings of 10 and 5, respectively.

(i) If the Pattern Generator is being used on a high-level loop circuit, set the HI-LEVEL SELECT switch to the position applicable to the type of loop circuit used.

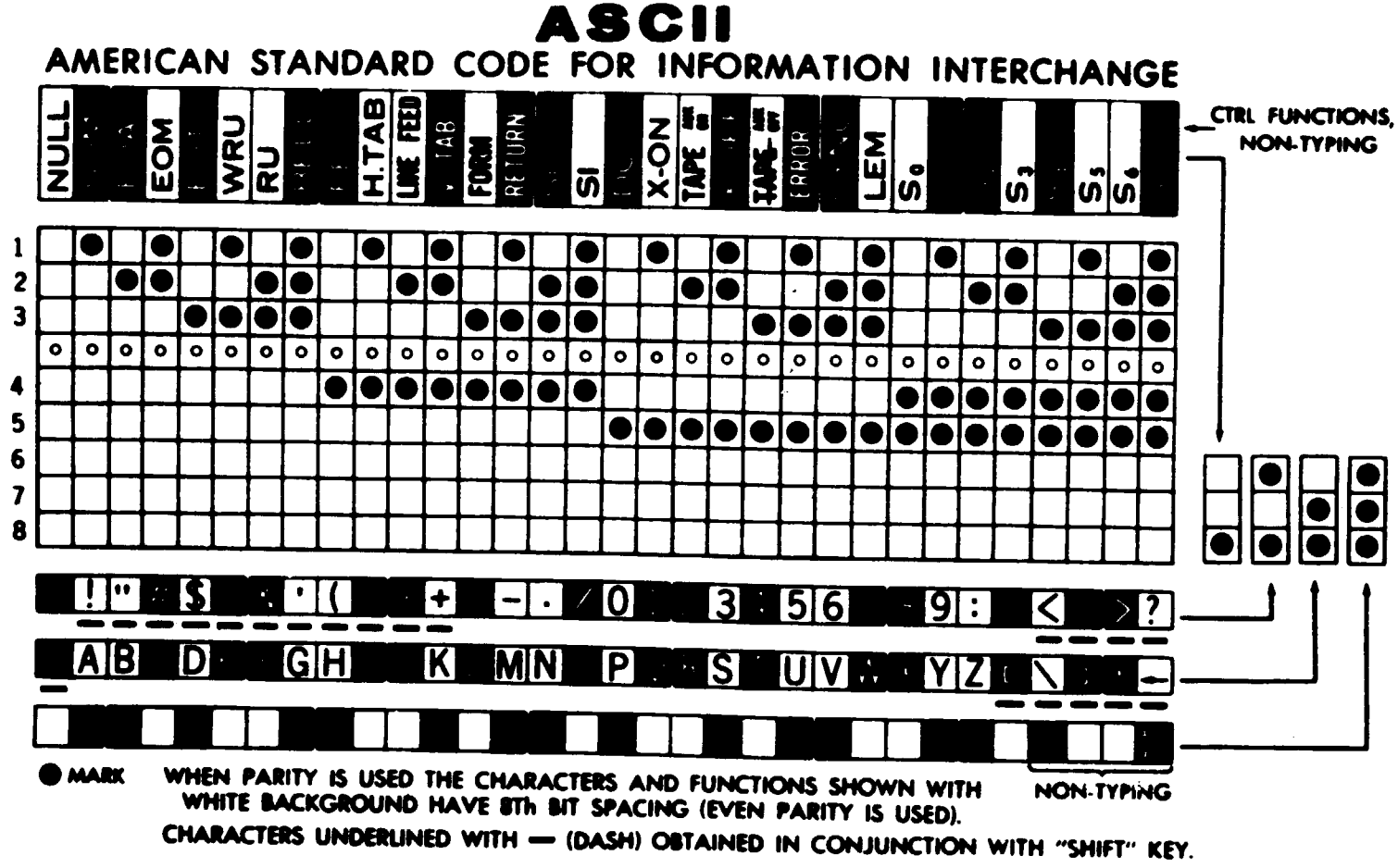


Fig. 16 - American Standard Code for Information Interchange

2.04 After the above control settings and manipulations have been made, the Pattern Generator will be operational for the conditions established. Changes may be made in most of the parameters of the output pattern while the unit is in operation. For example, the PERCENT distortion and TYPE distortion control settings may be changed at will.

3. PRINCIPLES OF OPERATION

(A) General

3.01 Pattern Generator operating principles are presented in two parts. The first part describes the various functional sections of the unit, using an over-all block diagram to depict interrelationships and main signal flow paths. The second part describes the circuitry and logic of the unit on an assembly basis. With some minor exceptions, each of the PC-card assemblies is functionally self-contained, so that it may be described separately in terms of the input and output signals that are processed. Simplified logic and block diagrams present the essentials of circuit operation without a point-to-point logic analysis.

(B) Over-All Functional Description

3.02 Fig. 17 presents a block diagram of the Pattern Generator showing the functional relationships between the major assemblies and the principal inter-assembly control signals and data paths. Power supply connections and the, numerous and complex switch control functions have been omitted for simplification. The signal interconnections shown in simplified form have been given functional titles to facilitate the description.

3.03 The time-base circuit furnishes the stable clock signal from which the various output data-bit rates and distortion-generating signals are derived. A crystal oscillator circuit is used for the basic clock; the crystal oscillator feeds a binary frequency-divider chain which provides the separate 100X clock signals for each data rate. The output frequency from the time-base circuit is 100 times the selected data-bit rate. The start control signal turns the time base on and off in the stepped mode of operation. In free-run operation, the time-base is always on.

3.04 The main purpose of the distortion generator circuits (PC-card A5) is to produce data shift pulses which are controllable over a relatively wide range in time so that known, adjustable amounts of distortion may be introduced on the output data patterns. These circuits also furnish the “tree time” pulses for zero-distortion output patterns or transitions. In all cases, the amount and type of distortion produced is selectively pre-determined by the front-panel control settings. A secondary purpose of the distortion circuits is to provide the unit with various clocking pulses (related always to the duration of the selected data-bit rate) which are used to effect switching, sampling, reset, and data-transfer functions within the Pattern Generator logic . The start control input to the distortion circuits is used to enable resetting of the distortion counting circuits. The data sense input is derived from the input to the

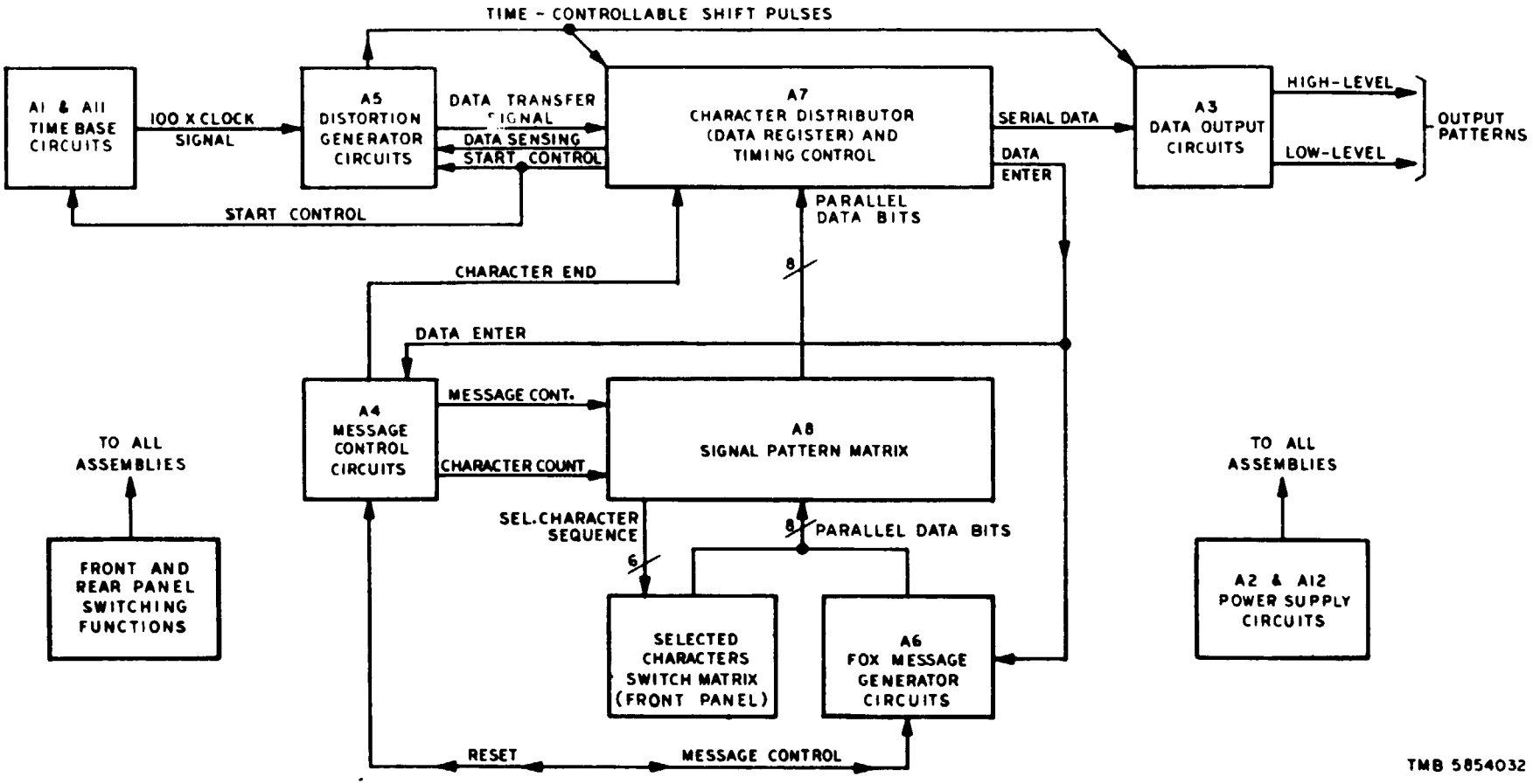


Fig. 17 - Over-All Block Diagram (Simplified) - Pattern Generator

last stage of the data register; its purpose is to sense the presence of a Mark or Space in this stage and thus signal the distortion circuit to produce a distortion or no-distortion shift pulse. The data-transfer signals include timing and gating pulses which are used in the synchronizing of data-transfer.

3.05 The character distributor (PC-card A7) contains a 10-stage shift register which performs a parallel-to-serial conversion of the message pattern data supplied from the signal pattern matrix. The last (eleventh) stage of the data register is located on PC-card A3; for this reason, the shift-pulse signal is shown applied to both A7 and A3. As character data-bits (in parallel form) are loaded into the register, they are shifted out serially to the output circuits on A3. For the random pattern and reversal pattern outputs, this parallel-to-serial operation is not used. These patterns are generated in serial form by the internal logic of the unit and applied to the serial input terminal of the shift register modules, whereupon it is directly clocked out. (This latter circuitry is not shown on this simplified block.) The data-enter signal is a timing pulse derived from gating circuits connected to the data register. This signal occurs each time the register has been emptied and is ready to receive the next character from the matrix. In the SELECTED CHARACTERS mode of operation, the data-enter signal is routed to circuitry on PC-card A4 to advance the character counter/sequencer, thereby causing the next character to be loaded into the data register. When the FOX message is being-generated, the data-enter signal, applied to A6, advances the FOX message character counter/sequencer to load the next FOX character into the data register. The character end signal applied to A7 is derived from gating circuits on A4. This signal, occurring at the end of each character or sequence, when the unit is being operated in the manual step or external step modes, halts further output until the next step pulse' is applied. In the free-run mode, the step pulse is generated automatically by the internal circuit logic; in the manual step mode, whenever the front-panel pushbutton is depressed; and, in the external step mode, by an external step signal.

3.06 The message control assembly (A4) contains miscellaneous circuitry which generates various control and timing signals required to effect the orderly sequencing and processing of the selected output patterns. The data-enter input from PC-card A7, occurring whenever the data register is empty and ready to receive the next character, generates the message control signal that is shown applied to the pattern matrix. This message control signal is an enable signal to the matrix that will allow a new character to be fed to the data register. Concurrent with producing the message control signal, the data-enter signal causes a character-counter circuit (four binary counter stages) to advance one count. This new character count, in BCD form, is fed to the pattern matrix. (This character-counter circuit pertains to the selected characters {switch matrix) only; the FOX circuits have a separate counter/sequencer.) A BCD-to-decimal decoder on the pattern matrix assembly receives this count and correspondingly advances one decimal step (to the next matrix character), thereby generating a signal pulse that causes the next selected character to be shifted into the data register. The message control signal is also fed to the FOX message assembly (A6), where it performs essentially the same function, in conjunction with the data-enter signal, as for the selected characters described above. The reset input from the FOX message assembly causes the message control signal to be reset at the completion of the FOX message.

3.07 The principal component of the signal pattern matrix PC-card (A8) is a multi-input diode/NOR-gate matrix. The purpose of this matrix is to provide a common input network to the data register for the various pre-programed character bit sources such as the front-panel switch matrix and the FOX message assembly. The matrix is driven by a group of NAND gates which are sequentially enabled by the character count and message control input signals. The first six gate positions are associated with the six selected characters programed via the front-panel switch matrix. As these first six characters are gated, each gated output pulse is fed to the front-panel selected character switch matrix, which develops the appropriate Mark/Space bit pattern for each programed character. This bit-pattern (in parallel form) is then applied to the data register via the NOR-gate matrix of PC-card A8. The output. data-bits of the FOX message assembly are applied to the NOR-gate matrix and data register on the same lines as the output of the switch matrix; however, these two signal patterns are always generated separately, thereby permitting the sharing of a common input connection to the matrix.

3.08 The FOX message generator circuit features a monolithic read-only memory (ROM) containing the pre-programed FOX message patterns for both the ASCII (8-level) and baudot (5-level) formats. This assembly also contains its own sequencing counter, stepped by the message control and data-enter input signals, for sequentially reading the output of the ROM. As the ROM is sequentially read, the output data-bits are applied to the signal pattern matrix. A gating circuit on PC-card A6, connected to appropriate points in the sequencing counter, develops the reset signal to the message control assembly when the predetermined count at the completion of the message has been reached.

3.09 The data-output circuits (PC-card A3) consist basically of two separate output circuits (high-level and low-level) driven simultaneously by the serial output of the data register. The high-level circuit provides the capability for keying polar, neutral, and Bell System Electronic Hub circuits at levels up to 130 volts. The low-level output produces a standard ±6-volt polar output per MIL-STD-188 or, by reversing the polarity, for RS-232 signaling. Output terminals are located at both the front and rear of the unit. Loop battery supplies for high-level operation must be externally supplied.

3.10 The power supply circuits (PC-card A2 and A12) provide regulated outputs of +15, - 15, and +5 volts to power the electronics circuitry of the unit. Over-load protection is provided by fuses in both the ac primary circuit and the individual dc output of each supply. The primary ac input circuit may be adjusted by strapping connections to operate from either a 115-volt or 230-volt source.

(c) Logic and Circuit Descriptions

Logic Definitions

3.11 Generally, the logic symbols used throughout this manual conform to the definitions and rules established by Military Standard 806B. The descriptive logic terms used in the text descriptions are defined as follows:

(a) A logical-0 signal or level equals approximately 0 volt. This logic level may also be referred to as being a “low. ”

(b) A logical-1 signal or level equals approximately +5 volts. This logic level may also be referred to as being a “high.”

(c) Triggering of logic elements such as flip-flops and counters is accomplished by negative-going transitions (+5 to 0 volts, or logical-1 to logical-0).

Time-Base PC-Cards A1 and A11

3.12 Logic and circuitry essentials of the time-base circuits are shown in Fig. 18. The stable crystal oscillator circuit is located on a small subassembly PC-card (A1A1) which connects to the main time-base PC-card. This circuit uses either the single A-range crystal (Y7) or one of six optional B-range crystals as the fundamental frequency source. The crystal oscillator output is applied to a frequency-dividing binary counter chair having ten different output division rates. Nine of these division rates follow the binary sequence from 1 to 256. The tenth division rate (for the bit rate of 50.0) is a factor of 192, obtained by altering the normal counting sequence via a feedback circuit. These ten output frequencies are all applied, together with the output from the external timing source shaping amplifier, to a gate selection network. This gating network contains one gate for each frequency; these gates are selectively enabled by positioning the 11-position BIT RATE frequency selector.

3.13 The selected gated output of the binary divider is applied to one input of the select A-range gate. This gate operates in conjunction with the B-range select gate and the range selection portion of the BIT RATE switch to select the A or B ranges of the time base. A ground input to either gate inhibits it and allows the other gate to be enabled. The B-range outputs of the time base are obtained by gating the ÷32, ÷16, or ÷1 frequency-division rates in association with the first six positions of the BIT RATE switch, which selects one of the six optional B-range crystals. The selected A-range or B-range frequency is applied to a flip-flop output stage which provides a further division factor of two. The output frequency from the time-base assembly is a factor of 100 times the indicated setting of the BIT RATE switch.

3.14 The start control input signal (SC) functions as an on-off control of the time base. The output flip-flop is clamped in the set state when the input is a logical-0 (SC), thereby preventing the flip-flop from being toggled by the input signal. At the same time, the SC signal resets the frequency-division countdown chain. When the start control signal is a logical-1 , the time-base circuit is enabled. In step mode operation, the time base is turned off between successive generation of characters or sequences.

Crystal Oscillator Circuit PC-Card A1A1

3.15 The time-base crystal oscillator is depicted in block form in Fig. 19. The common-base input stage serves as a constant-current reference source which is applied to one side of the differential amplifier. In addition, this input stage serves

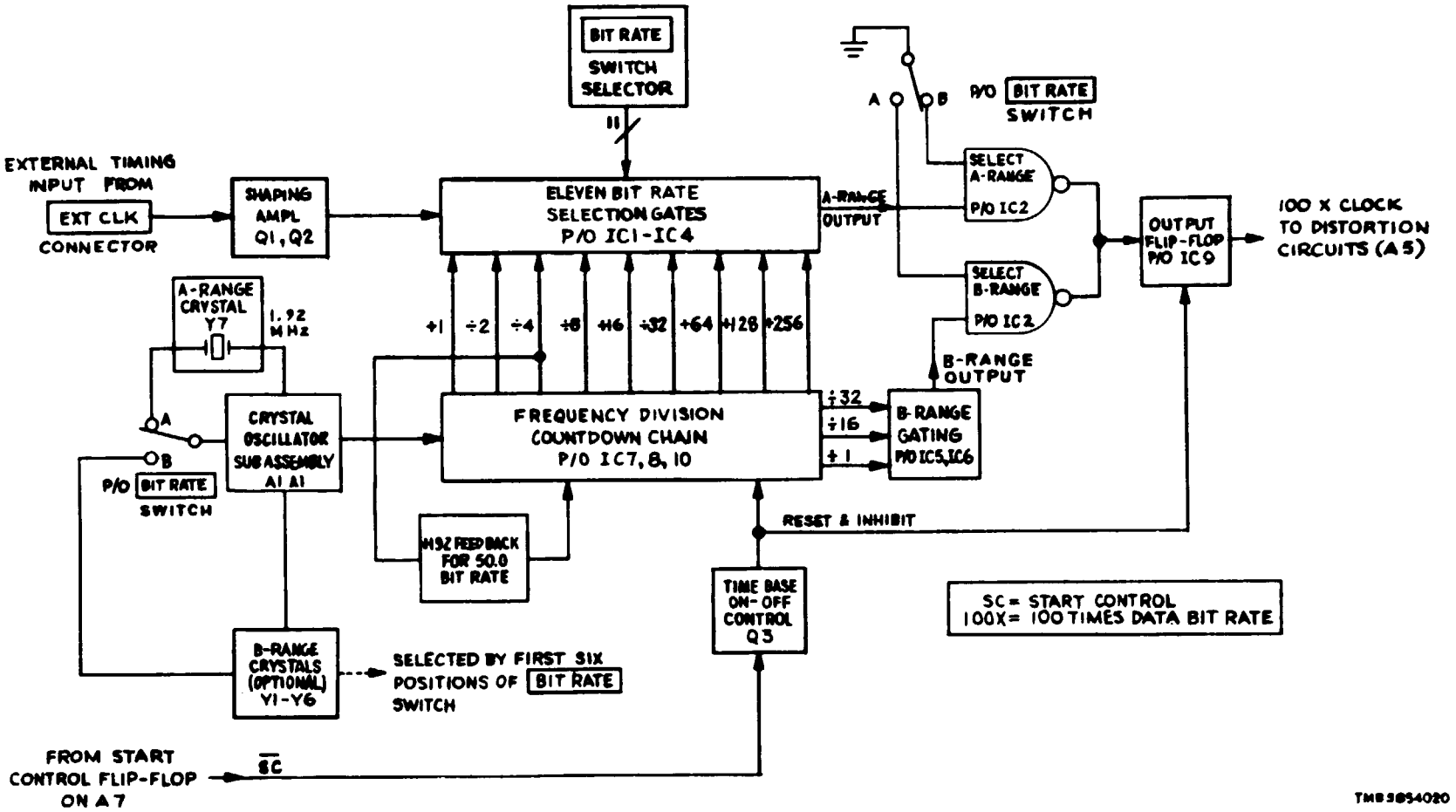


Fig 18 - Simplified Block/Logic Diagram - Time-Base Circuit

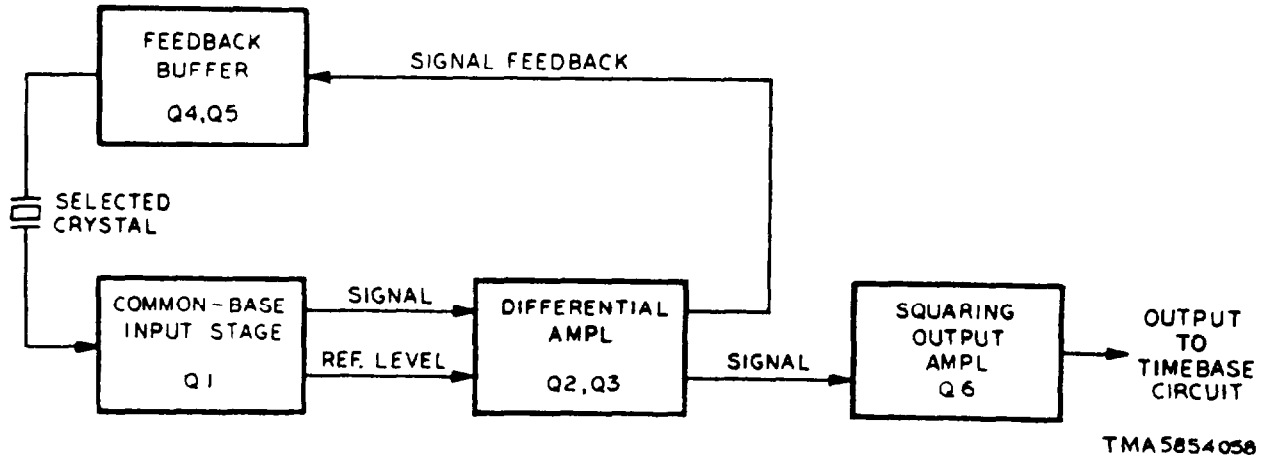


Fig. 19 - Block Diagram - Crystal Oscillator Circuit, Subassembly A1A1

as the input load for the selected crystal. The function of the differential amplifier configuration is to produce essentially uniform and reliable output levels over a wide range of crystal frequencies. The reference level provides compensation for variations in the outputs of the different crystals used.

3.16 Feedback is derived from the reference side of the differential amplifier and applied to the crystal via a 2-stage buffer consisting of cascaded emitter-followers (Darlington circuit). This buffer effects an impedance-transformation to provide the required low source-impedance for driving the crystal. The output squaring amplifier, fed from the signal side of the differential amplifier, produces a sharp-transition output waveshape.

Distortion PC-Card A5

3.17 The distortion circuit (Fig. 20) furnishes the time-controllable shift pulses used to clock the character bits out of the data register. Control of the time of shift pulse occurrence provides the means for introducing distortion on the transitions of the output signal. The input 100 X clock from the time-base, in association with two decade counters and BCD-to-decimal decoders, allows the data-bit to be divided into uniform increments in steps of 1 per cent and 10 per cent of the data-hi} period. An illustration of the data-bit period subdivision and its relevance to the distortion circuits is shown in Fig. 21. Two sample data-bits, encompassing three transitions, are shown. The data-bit transitions are produced by the shift pulse applied to the data register. These transitions, labeled A, B, and C, are shown on the first and second line. Between the transitions are the 10 per cent and 1 per cent subdivisions. Note that a complete span of 100 per cent extends from A to B and from B to C.

3.18 Taking transition B as an example, note that with respect to the direction of the time scale, shift pulses occurring to the left are early and those occurring to the right are late. Similarly, there is a period designated early and late around each shift pulse (transition) point. The maximum theoretical percentage that a given transition

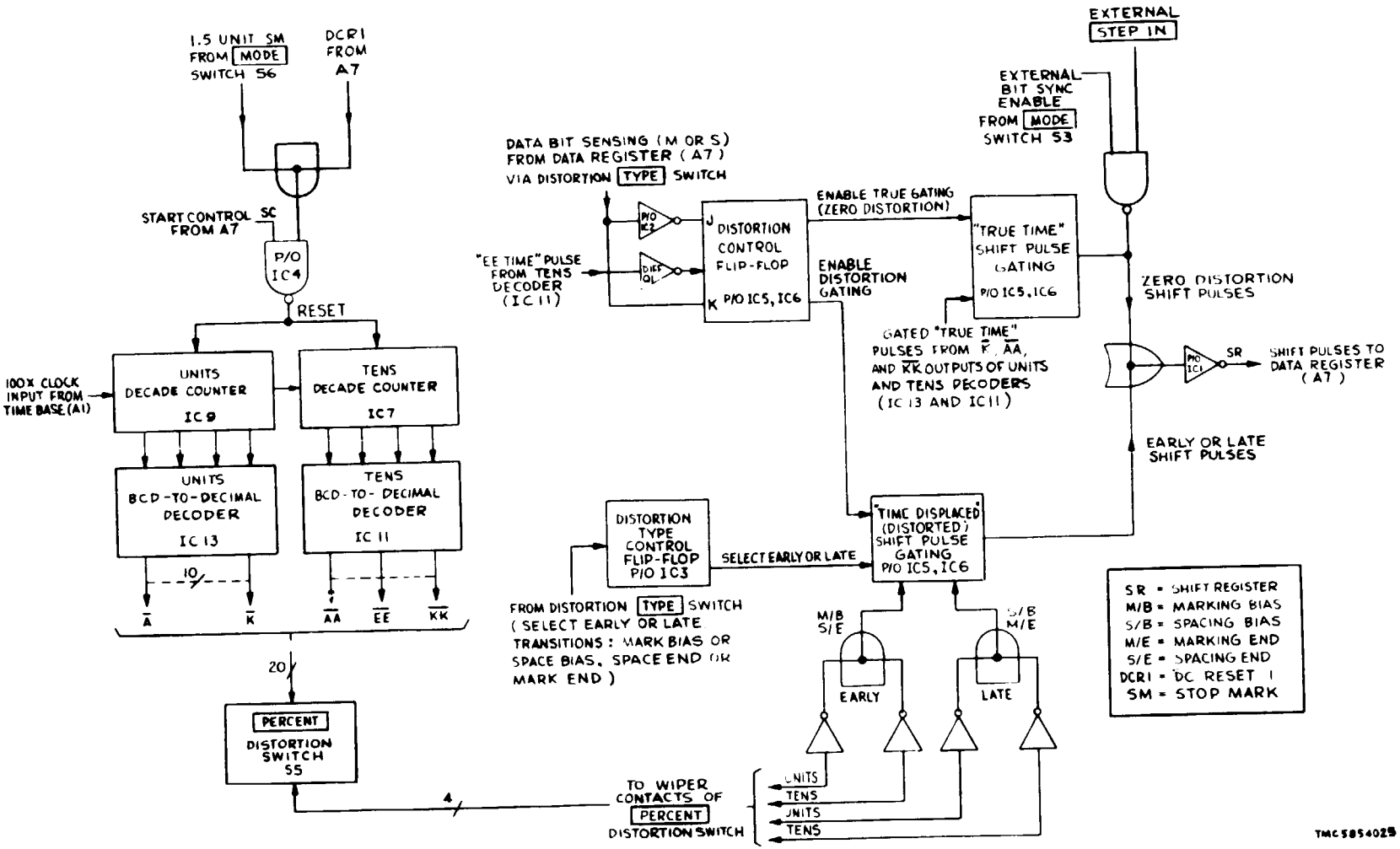


Fig. 20 - Simplified Block/Logic Diagram - Distortion Generator Circuits

will vary is 50 per cent; the maximum practical setting of the Pattern Generator is 48 per cent. The decade counter, BCD-to-decimal decoder combination counts uniformly from 1 to 100, then recycles and repeats the count as shown on line 3 of Fig. 21. Each count from 1 to 100 corresponds to one discrete point on the distortion scale. For instance, a count of 72 corresponds to an early shift pulse transition having 28 per cent distortion. The "true-time" or zero distortion transitions coincide with the zero count (reset) condition of the counter.

3.19 Referring again to Fig. 20, the outputs of the two BCD-to-decimal decoders, providing the units and tens outputs for every discrete count from 1 to 100, are applied to the various contacts of the dual-concentric BIT RATE switch. The wiper contacts of these switches, grouped in two pairs by units and tens, for early and late, are connected to a gating circuit controlled by the state of the distortion type control flip-flop. The state of this flip-flop, in turn, is established by the setting of the front-panel distortion TYPE switch. This entire early/late gating network is enabled or inhibited by the state of the distortion control flip-flop.

3.20 The distortion control flip-flop is the control element in the selection of "true-time" shift pulses or "distorted" (early or late) shift pulses. Depending on the state, either the "true-time" shift pulse gating network will be enabled and the "distorted" shift pulse gating network will be inhibited, or vice versa. Thus, only one "type" of shift pulse will be gated through at any one time to appear at the output as SR. The "true-time" pulses are derived by a gating network (not shown) connected to the zero (0%, 100%) outputs of the BCD-to-decimal decoders. The selection of "true time" versus distortion is determined by sampling the state of the next-to-last stage of the data register for a Mark or a Space. Since, by definition, the direction of the transition (Mark-to-Space or Space-to-Mark) establishes the classification (bias or end) of the distortion, sampling of this stage is necessary to provide the information needed to select a distorted or undistorted shift pulse. For example, if Marking bias distortion has been chosen, the shift pulse for all Space-to-Mark transitions must be made to occur early by the selected percentage. Thus, when a Mark condition is sampled in the next-to-last stage of the data register, the subsequent data transition will be initiated by an early shift pulse so that the transition from Space to Mark will be "distorted." Note that the data sampling logic level is applied to the distortion control flip-flop J-K inputs at opposite logic levels by inverting the input to the J terminal. In this way the flip-flop is enabled for a change of state by the EE toggle pulse. The toggling pulse for this flip-flop occurs at "EE" time; this is at the center of the data-bit (corresponding to a count of 50).

3.21 When an external source is used to clock the output data from the Pattern Generator, this stepping signal is routed to the output of this assembly via a NAND-gate enabled by the setting of the MODE switch to the EXTERNAL-BIT SYNC position. At the same time, both the "true time" and the "time displaced" gating networks are inhibited by a logical-0 derived from this same MODE switch setting.

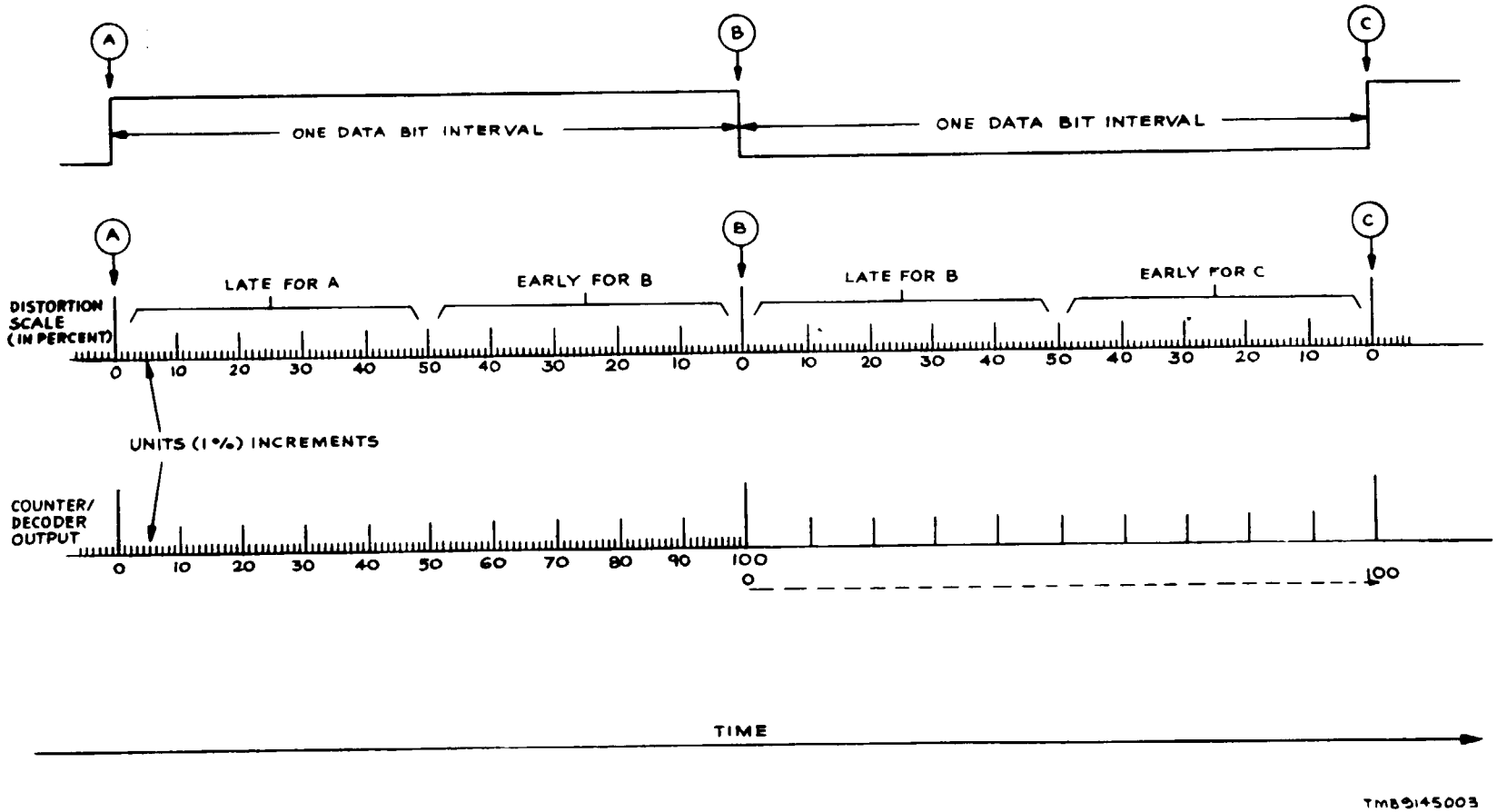


Fig. 21 - Distortion Circuit Bit Division and Timing

Data Register PC-Card A7

3.22 The Pattern Generator data register contains a total of 11 stages to encompass the maximum bit-length signal pattern generated; this maximum-length signal would be an 8-bit start-stop code having a 2.0 unit stop-Mark. Ten of the stages are contained on PC-card A7 (see Fig. 22); the eleventh stage is located on PC-card A3 (Fig. 26). Input data from the pattern matrix, some of which are routed via the PATTERN switch, are parallel-loaded into the register by the read pulse which is generated when the previous content of the register has been shifted out, The number of active data-bits that are applied to the register depends on the format of the selected pattern. In the case of a 5-unit start-stop code having a l-unit stop-Mark, the total number of bits is seven. Data patterns are shifted out of the register by the SR signal originating from the distortion circuit (PC-card A5), but routed via an inverter circuit on PC-card A3 .

3.23 Loading of the register is accomplished by a read pulse which gates each character into the register in parallel form. This read pulse is derived from the data-enter signal and a clock pulse ($\overline{J}$ output) from the units decoder of the distortion circuit. The data-enter (DE) signal is generated when every stage of the register is in the Space condition; that is, when the last Mark (the stop-Mark) of a start-stop character has been shifted out of the register, the register is empty and is ready to receive the next character from the pattern matrix. Thus, the "all Space" condition, detected by a gating network which senses each stage of the register, enables a change of state of the data-enter control flip-flop when the D clock pulse from the distortion circuit is applied. It should be noted that the D clock which toggles the flip-flop occurs a short time before the $\overline{J}$ clock which provides the read pulse. As soon as a new character is in the register, the "all Space" condition no longer exists and the enable input is removed. When the next D clock pulse arrives, the data-enter control flip-flop is reset, since a fixed +5-volt enable is applied to the other input. This removes the data-enter signal.

3.24 The foregoing sequence of events, involving the loading of a new character into the data register, takes place during the first half of the start-Space bit interval of the new character. In this way, successive start-stop characters are generated with no breaks for recycling and loading the register. The "last Mark" (LM) output signal is developed when the last Mark of the start-stop character is in the final stage of the register. This LM signal is applied to PC-card AS, where it is combined (gated) with the EE clock pulse from the distortion counter to perform various timing and clocking functions (see Fig. 20). One of the uses of this combined LM and EE signal is to perform a reset function in the start-stop mode of operation when the stop-Mark duration is a 1.5-bit interval. This $\overline{LM \cdot EE}$ signal is used to develop the DCR1 (dc reset 1) signal via a gating circuit on PC-card A7; this DCR1 signal is operative only in the start-stop mode and, in time, it is coincident with the $\overline{LM \cdot EE}$ signal. When the 1.5-unit stop-Mark is being produced, a 2.0-unit stop-Mark is initially loaded into the register (see Fig. 22). However, the distortion counter is reset in the middle of the second of these two stop-Mark intervals by the DCR1 signal gated with the enable level derived from the 1.5 position of the MODE switch (see Fig. 20). In other words,

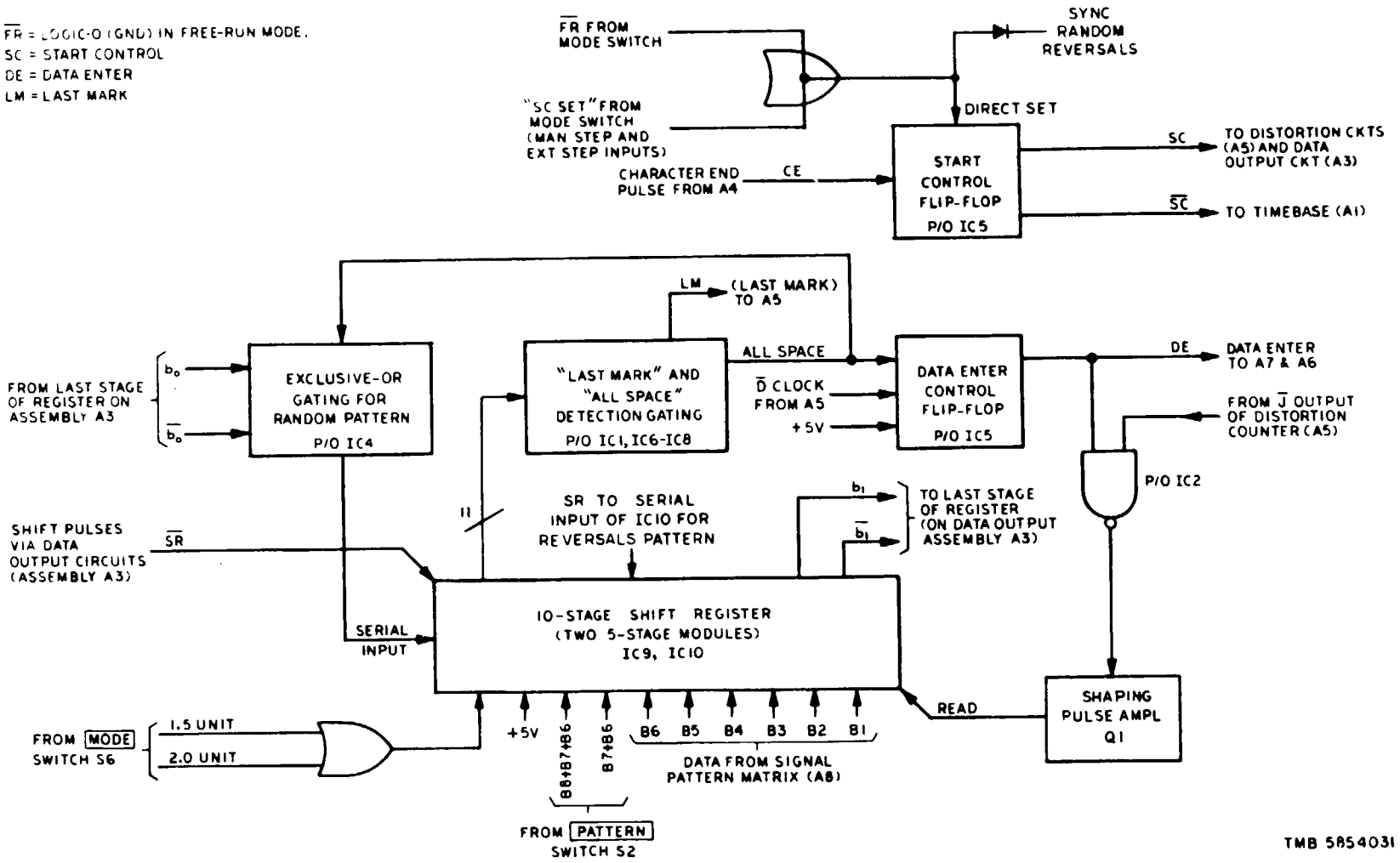


Fig. 22 - Simplified Block/Logic Diagram - Data Register Circuit

when the “last Mark” condition occurs, the reset signal is developed one-half a bit interval later, thus cutting the second of the two stop-Marks in half. This reset signal to the distortion counters is gated with the SC (start control) signal which, in the case of start-stop operation, is an enabling logical-1 at this time. The SC signal is explained in further detail in 3.27.

3.25 Synchronous operation is similar to start-stop in that the characters are parallel-loaded and serially shifted out of the register, but there are no start-Spaces or stop-Marks between the data information bits. Therefore, the last Mark and all Space detection circuits operate in a different manner than for start-stop. In synchronous operation, the “last Mark” detection gating is arranged to detect a Mark in the next-to-last stage of the register, with all the remaining stages containing Spaces. As previously described, start-stop operation detects the last-Mark in the last stage of the register. In synchronous operation, an extra Mark is loaded into the register at the end of each group of data-bits; its purpose is to serve as an “indicator Mark” to identify the end of each group of synchronous character bits. This “indicator Mark” never gets out of the register to appear as an output bit as does the stop-Mark in a start-stop character. When this synchronous indicator Mark is in the next-to-last stage of the register, it signifies that the last bit of the synchronous character is in the last stage of the register and is thus being transmitted. At this time, the remaining stages contain Spaces, and the conditions for detection of the end of the synchronous character are satisfied; i.e., the indicator Mark is in the next-to-last stage with the subsequent stages all Spaces. Upon detection of this condition, the indicator Mark is reset to a Space, whereupon the next synchronous character is loaded into the register, with a new indicator Mark following the last character bit. This detection and reloading process takes place in each case while the last bit of the previous synchronous character is “on the line;” i.e. , in the last stage of the shift register.

3.26 In the random pattern and reversals modes of operation, the data register is not loaded and emptied as described above. The random pattern is produced by a closed feedback loop which operates through an exclusive-OR gating circuit into the serial input terminal of the first shift register module (IC9) . For reversals patterns, the SR output of the distortion circuit is propagated directly through the second half of the register by feeding back a sample of this signal, via the functional switching of the PATTERN switch, to the serial input terminal of the second shift register module (IC10).

3.27 The start control flip-flop contained on this assembly functions as an “on-off” switch in the character and sequence step modes of operation. In the free-run, synchronous, random, and reversals modes of operation, a direct set input is applied which keeps the flip-flop set. In the set state, the SC and $\overline{SC}$ outputs are applied as enabling signals to the distortion circuit (A5) and the time base circuit (A1), allowing these circuits to perform their normal functions. In the step modes of operation, the start control flip-flop is set by the “SC set” signal, either through actuating the front-panel RELEASE switch or by applying a pulse from an external source to the rear-panel STEP IN terminals. These stepping signals are routed via the MODE switch. When

thus set, the Pattern Generator produces a single character or a single character sequence output, depending on which has been selected. At the end of each single character or single sequence generated, the character end (CE) signal, generated on PC-card A4, toggles the start control flip-flop to the other state, thereby "turning off" the unit. While in this "off," the SC signal applied to A3 puts the last stage of the data register in the Mark state, thereby producing a "steady Mark" output from the Pattern Generator during the intervals between step pulses.

Signal Pattern Matrix PC-Card A8 (See Fig. 23.)

3.28 The circuitry on this assembly consists of three principal sections: the BCD-to-decimal decoder, the character-sequencing 2-input NAND gates, and the NOR-gate/diode matrix. The decoder translates the BCD output of the character counter on A4 into a sequential decade count of from 1 to 10. The 2-input NAND-gates are arranged into three main groups as follows: the first six gates are associated with the six programmable characters selected by the front-panel switch matrix; the next five gates (C7 through C11) are used in generating the final characters of the 5-level (baudot) FOX message; the third group consists of five gates (C7 through C11 again) used in generating the ending of the 8-level (ASCII) FOX message. Finally, there is the C12 (character 12) gate used only in the S-level (baudot) FOX message. As the BCD input to the decoder is decoded, the sequential output applies activating signals to gates 1 through 10. An enabling level for these gates is derived from the MC (message control) signal from A4. It should be noted that the MC signal is used in the control and transfer of data from the FOX message circuit on A6 and the selected character switch matrix, via the A8 pattern matrix circuit to the data register. The MC signal is explained in the next part of this section. The first six gates activated cause the programed content of the selected characters switch matrix to be sequentially parallel-shifted to the data register via the NOR-gate/diode matrix.

3.29 For a given FOX message format, only one group of the message ending gates will be enabled. This selective enabling is accomplished by a gating network in association with the PATTERN switch-derived baudot and ASCII signals and the M C signal from A4. After the first six characters are enabled, the next five characters (in the selected format) are sequentially produced. However, in this case, the outputs of the C7-C11 gates feed the NOR-gate/diode matrix directly. Character 11 is obtained from a separate gating circuit on A4 (connected to the character counter on that same assembly), since a maximum of only ten outputs is available from the BCD-to-decimal decoder. The character 12 signal is obtained in a similar way.

3.30 In the ASCII 8-level code format, the eigth bit position is designated as a parity information bit. The Pattern Generator provides strapping connections for establishing the mode of parity (odd or even) or for deleting the parity information and substituting a constant Mark in this bit position. The eighth ASCII data-bit is routed to the data register via a gating network controlled by the strapping connections.

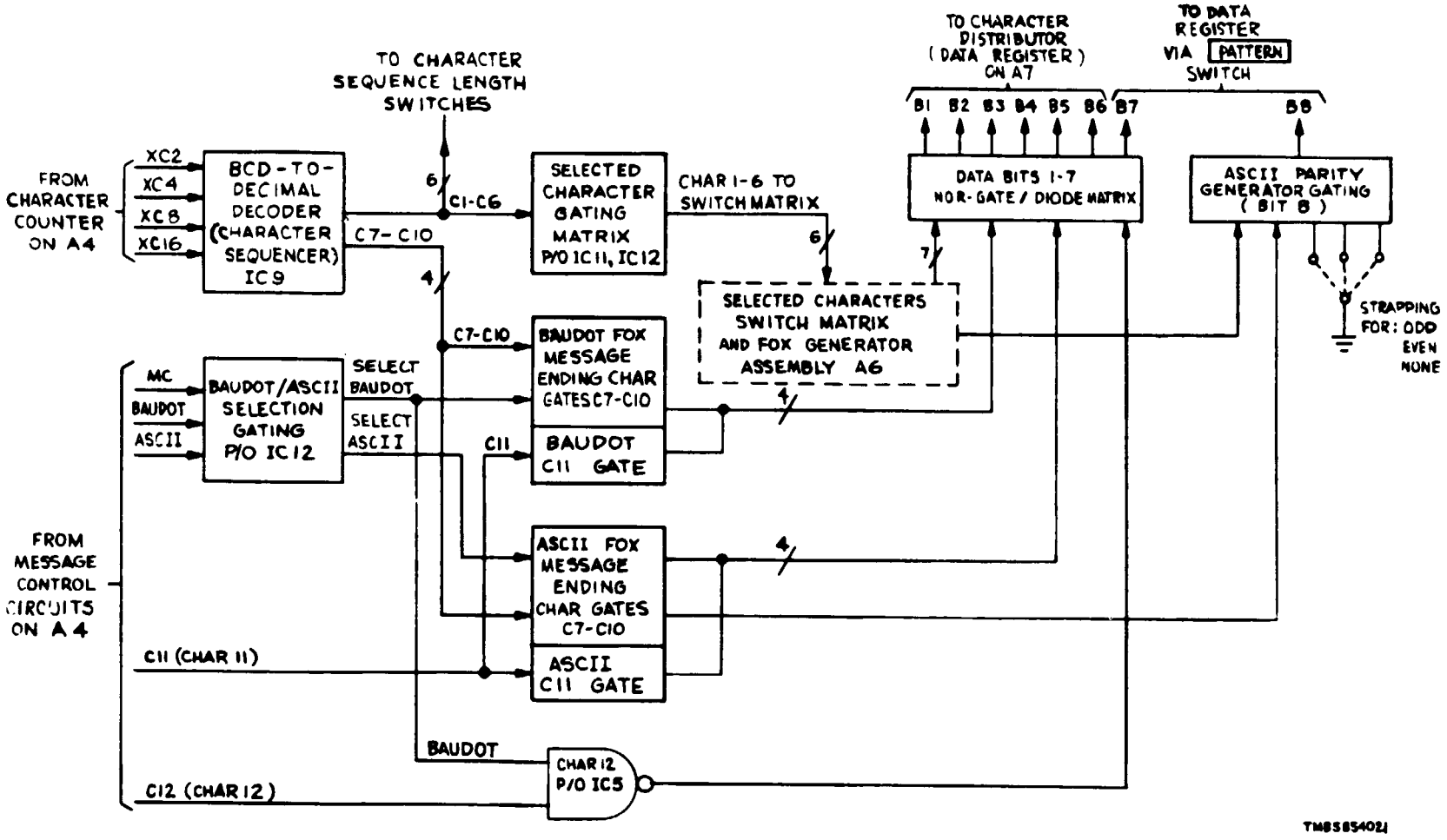


Fig. 23 - Simplified Block/Logic Diagram - Signal Pattern Matrix

Message Control Circuits, PC-Card A4 (See Fig. 24.)

3.31 This assembly consists of various counting, gating, and flip-flop circuits used in controlling and sequencing the selected output patterns. The selected character-sequencing counter provides the counting sequence (up to 12) that sequentially activates the pattern matrix gates which, in turn, load the six front-panel programmable characters and the FOX message endings into the data register. The output of this counter, in BCD form, is decoded by circuitry on A8 for the first 10 counts. The remaining two counts, 11 and 12, are developed by the CHAR 11 and CHAR 12 gating circuits on A4. The message control flip-flop is the key control element of this circuit . Operation of the circuit will first be described for the case of FOX message generation. In one state of the flip-flop, the selected character sequencing counter is activated and the selected character gate matrix is enabled; in the other state, the FOX message 6-stage sequencing counter on A6 is activated. A data-enter clocking pulse is applied to the flip-flop with each new character. The state assumed by the flip-flop will be determined by the logic levels applied to the J and K inputs. At the end of the ROM FOX message sequence, the JMC signal goes high and allows the next data-enter signal to toggle the flip-flop, thus switching to the selected character-sequencing counter on A4. At the end of the selected character portion of the FOX message, the C12 signal (derived by gating selected points in the counter) goes high, allowing the flip-flop to change state and reactivate the ROM counter on A6.

3.32 Operation of the circuit for the selected character patterns will now be described. When either the 6- or 7-level selected character position of the PATTERN switch is being used, the message control flip-flop remains in the set state via a direct set input. For the 5- or 8-level code patterns, the message control flip-flop is left free to be toggled for the purpose of switching to the ROM to generate a carriage-return/line-feed signal after 72 characters have been generated. In selected character operation, the sequencing counter is reset by the C6 signal from gate G-1 instead of the transition being derived from the change of state of the message control flip-flop. Since there is a maximum of six programmable selected characters, the counting sequence needs to extend only to six instead of twelve. Gate G-1 is disabled in either of the two FOX message positions of the PATTERN switch. Thus, the counter is reset every six characters only in selected character operation.

3.33 The C6 signal, which resets the sequencing counter, also steps the 72-character counter. This counter is used in the generation of an automatic carriage-return/line-feed signal after each sequence of 72 characters has been generated (in 5- or 8-level code patterns only). The counter, normally a 16-count configuration, is arranged to count to 12 (signifying 72 characters, since the C6 input pulse occurs every six characters) by connecting the inputs to gate G-3 to those points of the counter that will activate the gate at the count of twelve. When gate G-3 is activated, it generates the equivalent of a Cl 2 signal, thus causing the message control flip-flop to change state and thereby activate the ROM FOX message circuitry on A6. The pre-programed carriage-return/line-feed (CR/LF) sequence is contained in the initial portion of the ROM. This automatic CR/LF feature is optionally enabled or disabled by the rear-panel CR/LF switch which controls gate G-3.

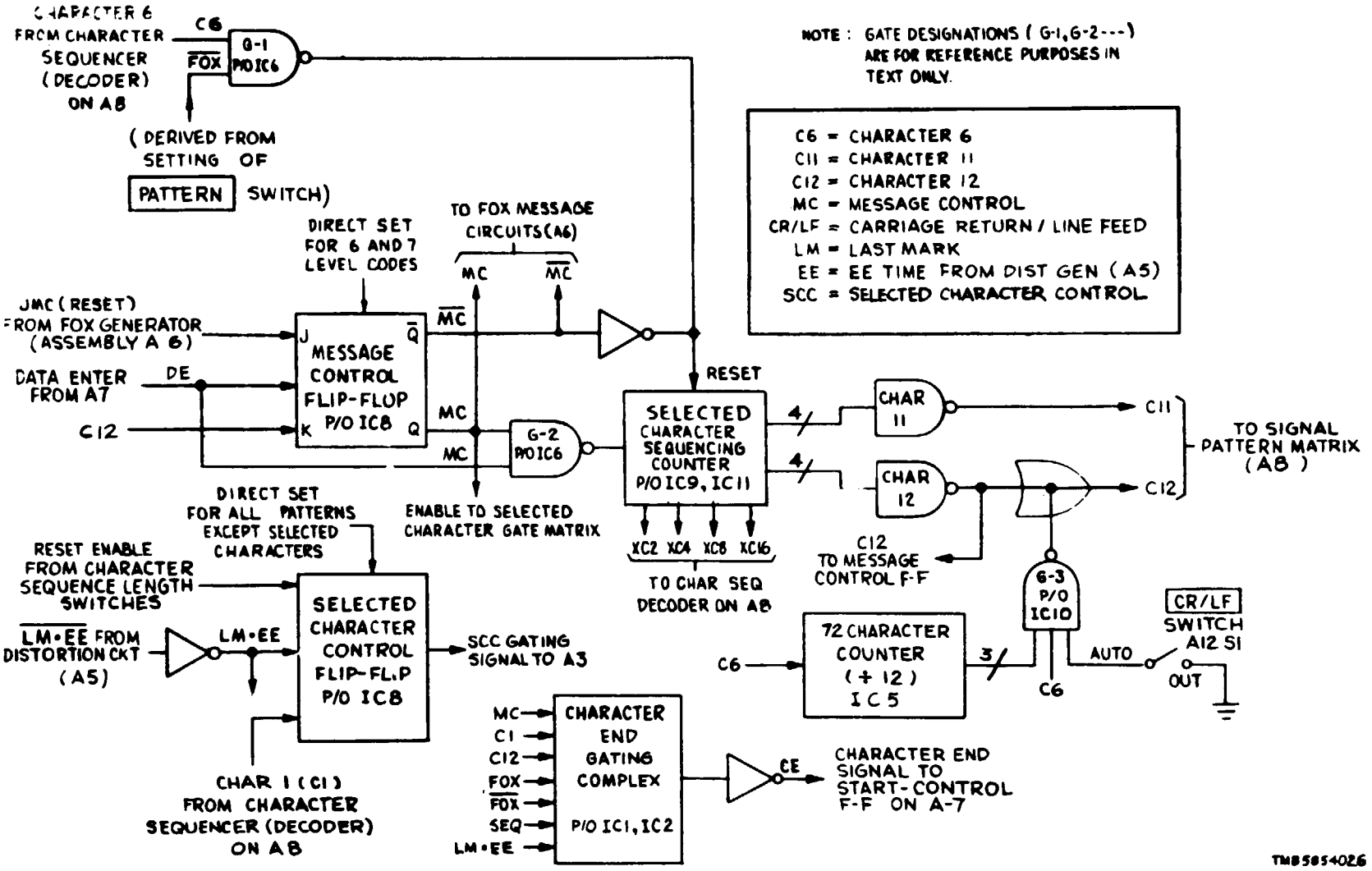


Fig. 24 - Simplified Block/Logic Diagram - Message Control Circuits

3.34 The selected character control flip-flop, operating independently of the other circuitry on this assembly, is used in conjunction with the front-panel CHARACTER SEQUENCE LENGTH switches to control the number of selected characters generated in each message sequence. The output of this flip-flop controls the gating of the output of the data register. When the flip-flop is in the set state, the character control gate (located on A3) is enabled and the output of the register is gated through to the output circuits, For all patterns except selected characters, a direct set input keeps the flip-flop in the set state. When this flip-flop is reset, the gate is disabled and the output signal becomes a steady Mark. Thus, if the number 3 CHARACTER SEQUENCE LENGTH switch has been depressed, only the first three of the six programmable selected characters will be generated. At the end of the third character, a reset enable signal, derived from the character sequencer (on A8) and routed via the number 3 CHARACTER SEQUENCE LENGTH switch, will reset the selected character control flip-flop. The flip-flop will remain in this state, producing a steady Mark output signal for the three remaining character intervals, until it is returned to the set state by recurrence of the character 1 enabling input at the time the sequencing counter is reset. The LM EE clocking pulse to the flip-flop is developed during each character cycle when the last Mark is in the last stage of the data register. This $LM \cdot \overline{EE}$ transition occurs at the center (50% point) of the last Mark bit.

3.35 The character end gating complex contains three multi-input gating circuits that function to generate the character end (CE) signal when the unit is operated in the external step or manual step modes. This character end signal, when generated, is applied as a toggle input to the start-control flip-flop to cause this flip-flop to "turn off" the unit. Whenever a single character or a sequence of characters has been generated in the step mode of operation, the CE signal resets the start-control flip-flop, which, in turn, causes the unit to emit a steady Mark output until the next step pulse initiates another character or sequence cycle.

FOX Message Generator Circuits, PC-Card A6

3.36 The heart of the FOX message generator circuits (see Fig. 25) is a read-only memory device (ROM) consisting of a single MSI integrated-circuit module. This single device contains the bulk of the FOX message in both the 5-level and 8-level code formats. Only the last two groups of characters, the 6-character station identification code and the word TEST, originate outside the ROM. These last portions of the FOX message are derived from the SELECTED CHARACTERS switches and from separate gated, sections of the pattern matrix assembly (see 3.27). The ROM is read, character-by-character, by applying a progressive binary count (up to 63) to six counter input terminals. The output is taken from eight terminals for the ASCII format and from the first five terminals in the case of the baudot (5-level) format.

3.37 The 6-stage sequencing counter consists of six flip-flop circuits connected in a straightforward binary counter configuration. This counter is enabled when the MC signal applied to gate G-2 from the message control flip-flop on A4 is high (logical-1). At this time, the selected character counter on that same assembly is inhibited by the logical-0 state of the MC output. Thus only one of these two sequencing counters is operative at a time, as established by the state of the message control flip-flop. The

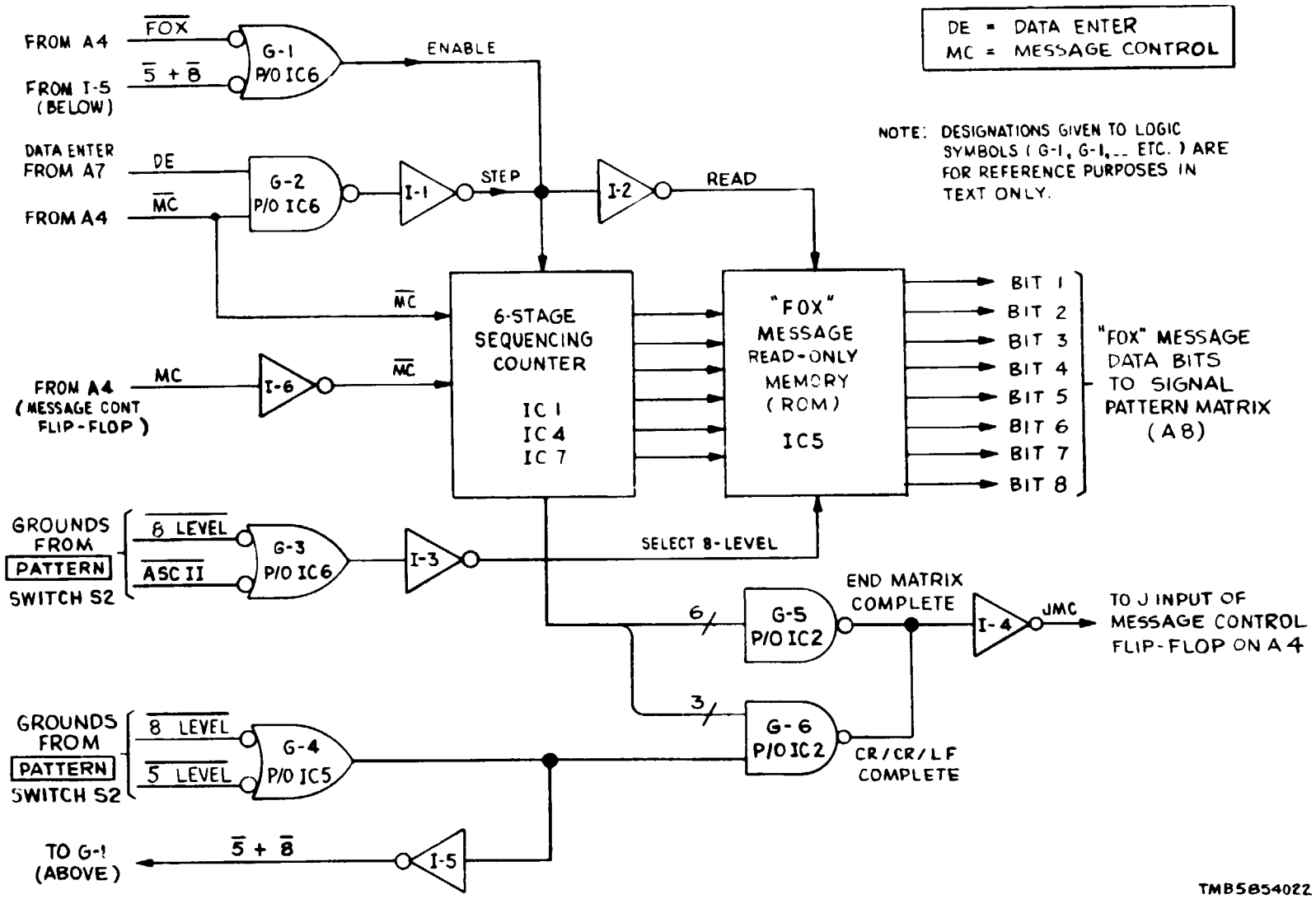


Fig. 25 - Simplified Block/Logic Diagram - FOX Message Generator

MC levels applied to the counter serve also to reset the count to zero at the beginning of a new message. With gate G-2 enabled by the high $\overline{MC}$ signal, signal, the data-enter signal is gated and inverted to clock the counter. A logical-1 level at the output of gate G-1 is necessary to enable the counter to be stepped. This enable input from gate G-1 is applied whenever the PATTERN switch is set to either of the FOX positions or to the 5-level or 8-level selected character positions. This circuitry is enabled for the 5-level and 8-level selected character positions of the PATTERN switch so that the carriage-return/line-feed characters may be generated after each cycle of 72 characters. It should be noted that the first four programed characters of the ROM contain a carriage-return/line-feed sequence; in generating the automatic CR/LF after 72 characters in 5- and 8-level modes, this portion of the ROM is used, and then reset.

3.38 Concurrent with stepping the sequencing counter, a read pulse is developed for the ROM. This read pulse gates the character bit pattern out of the ROM in parallel form. The selection of 5-level or 8-level code format is made by the signal applied to the ROM via gate G-3 and inverter I-3. A ground signal (logical-0) is applied to G-3 when the PATTERN switch is set to either the 8-level selected character position or the 8-bit FOX message (ASCII) position. The resultant logical-0 applied to the ROM causes the 8-bit output pattern to be generated. With a logical-1 (high) applied to this ROM input, the 5-bit output pattern (baudot) is generated.

3.39 The remaining circuitry on this assembly, gates G-4 through G-6, is used in developing a reset signal to terminate the FOX message sequence. That is, when the ROM content has been read, the enabling input levels (MC and $\overline{MC}$) which initiated operation are removed by changing the state of the message control flip-flop on A4. Gate G-5 has 6 inputs, one from each stage, to detect the full-count state of the counter. When the counter reaches this count at the end of the FOX message sequence, an output transition is developed which is applied as a reset to the message control flip-flop. Similarly, gate G-6, with 3 inputs from the counter, causes this same reset signal, but at a different count. This time the reset occurs at the count of 4, when the carriage-return/line-feed portion of the ROM message content has been generated. This latter case applies only to the 5-level and 8-level selected character positions of the PATTERN switch and only if the circuitry has been enabled by the rear-panel CR/LF switch (see Fig. 23) . Gate G-4 furnishes an enable input to gate G-6 when the PATTERN switch is set to either of these positions . Inverter I-5 develops a logic signal for use as an input to gate G-1.

Data Output Circuits, PC-Card A3

3.40 A simplified block diagram of the Pattern Generator output circuits is shown in Fig. 26. The output of the final stage of the data register is applied to one input of the character control gate. This gate is enabled or inhibited by the SCC signal output of the selected character control flip-flop on A4 (see Fig. 24). Whenever the gate is inhibited, the output level of the gate is a logical-1 (high); this produces a Mark signal at the output terminals of the unit. For all operating patterns except selected characters (5-level through 8-level), this gate is held in the enable condition by keeping the flip-flop in the set condition. In selected character operation, the gate receives an inhibit level at the completion of the programed number of selected characters (one through six) established by the front-panel CHARACTER SEQUENCE LENGTH switches.

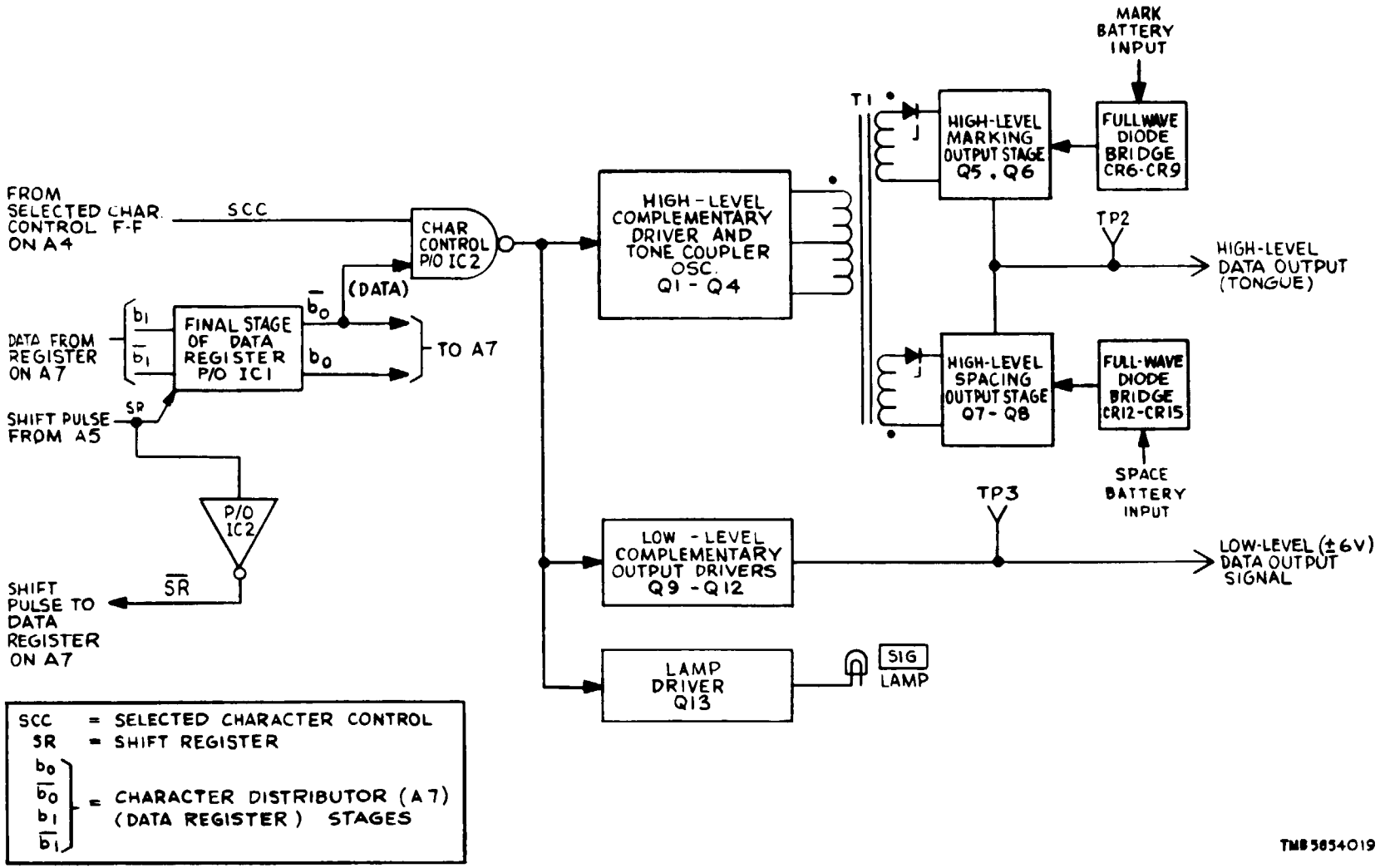


Fig. 26 - Simplified Block/Logic Diagram - Data Output Circuits

3.41 The output of the character control gate is applied simultaneously to the high- and the low-level output driver stages; in addition, the front-panel SIG indicator lamp driver circuit is activated. The SIG indicator lamp illuminates when the output signal is a Mark. The high-level driver stage consists of a pair of complementary transistors connected in a push-pull configuration driving the center-tapped primary of transformer T1. The common return (the center-tap lead of T1) contains a unijunction-oscillator operated switching circuit which functions in a manner similar to a tone coupler to transfer the dc data-bits to the output stage via the transformer, thus providing dc isolation. Each output stage contains high-voltage switching transistors operating in an open-circuit/saturated condition, analogous to relay contacts. The polarity of the secondary windings is arranged so that only one circuit is switched into conduction at a time.

3.42 Loop batteries for high-level operation are connected to the output (relay) circuit through a full-wave diode bridge circuit on each side of the circuit. This bridge circuit makes it unnecessary to label the loop battery connection points with polarity signs (+ or -). Thus, battery connection is simplified and the possibility of damage or destruction to circuit parts, due to improperly connected loop batteries, is eliminated. For example, when setting up operation for a positive Mark, the operator or installer simply connects the Mark (M) terminal to the positive terminal of the loop supply. The details of these connections, and the necessary precautions, are fully explained under (E) Installation in Section 1 of this manual.

Power Supply Circuits, PC-Card A2

3.43 Operating voltages for the Pattern Generator circuits are obtained from three separate, but interrelated, regulated power supplies furnishing outputs of +15 volts, -15 volts, and +5 volts. The essentials of these power supplies are depicted in the functional block diagram of Fig. 27. One power transformer is used for the three supplies; full-wave rectification, in conjunction with center-tapped secondary windings, is also used in all three cases. Rectifiers CR3 and CR4 are connected in opposite polarity to the other rectifiers, as required to furnish a negative 15-volt output with respect to ground. The Zener reference diode for the +15-volt supply is also used as the reference source for the +5-volt supply. The remaining circuitry of these supplies is conventional in configuration and in circuit details.

3.44 The 5-volt power supply employs a series-regulator circuit with a protective over-voltage circuit connected across the output terminals. The 5-volt supply is the operating power source for all the integrated-circuit modules. For this reason, prevention of an over-voltage condition at the output of this supply is essential; an over-voltage condition would probably result in the destruction of many of the integrated-circuit modules in a small fraction of a second.

3.45 The over-voltage protection circuit functions in the following manner (see Fig. 28). Under normal operating conditions, Zener diode VR3 is back-biased (nonconducting), thereby keeping transistor Q9 in a cut-off state. The SCR (CR7) is thereby also nonconducting, since its gate electrode is at ground (0-volt) potential when Q9 is nonconducting. Any over-voltage condition of greater than 7.5 volts will cause Zener

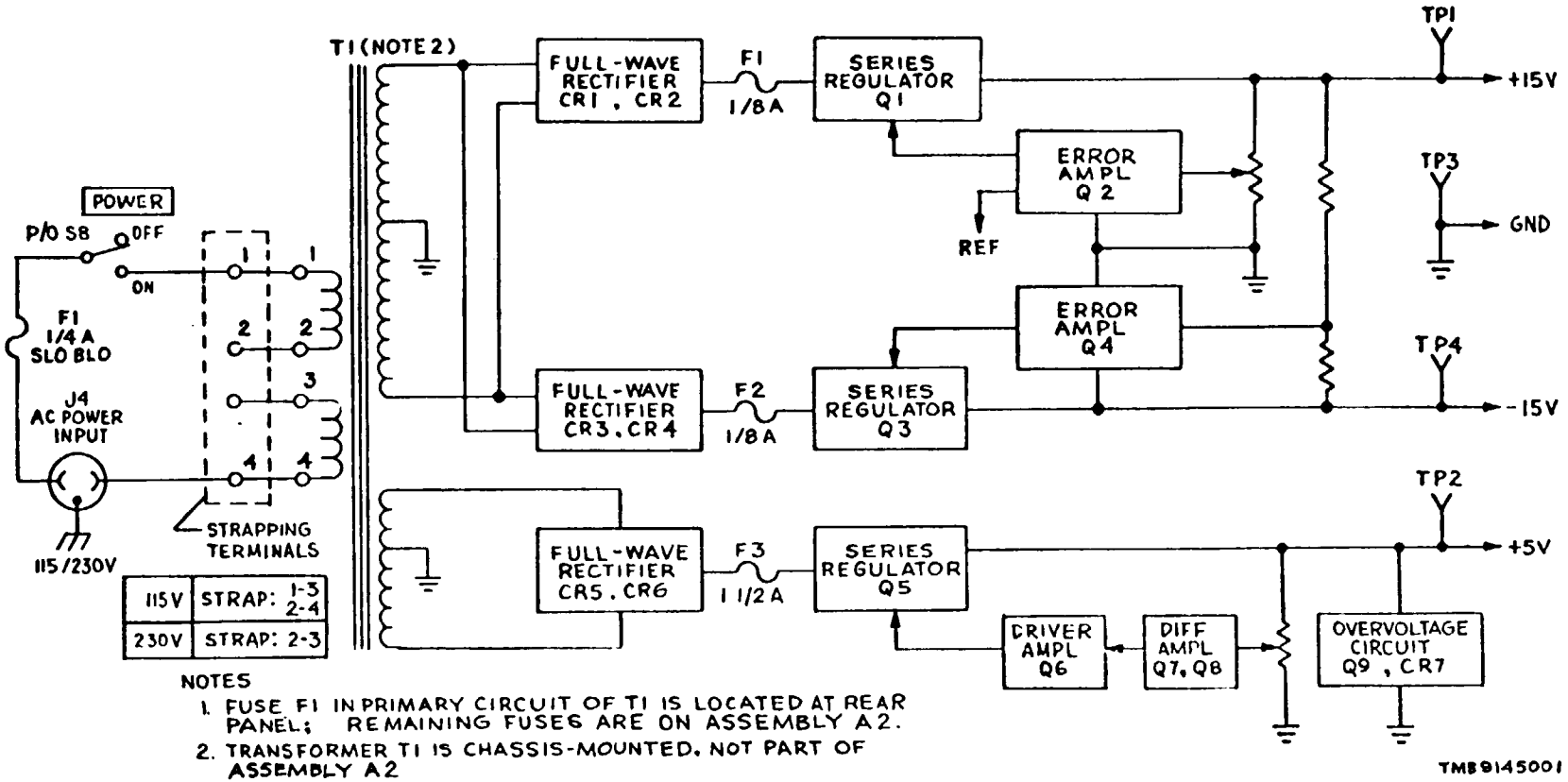


Fig. 27 - Simplified Block Diagram - Power Supply Circuits

VR3 to break down and will thereby turn on both Q9 and CR7 to full conduction. The fully conducting SCR effectively short-circuits the power supply and blows dc fuse F3, which is located at the input to the series-regulator stage. This removes the supply from service. The circuit operates automatically and is self-resetting after the fuse is replaced and the fault condition remedied.

3.46 Each of the three supplies contains a series dc fuse for the purpose of short-circuit protection. It should be noted that a momentary short circuit will not normally cause a fuse to fail; the short-circuit condition must be a sustained one in order to blow the fuse. In either case, full protection is provided for all circuit components.

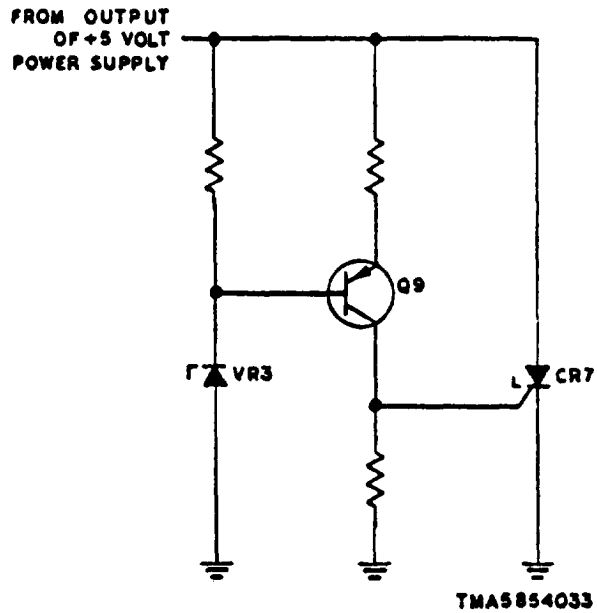


Fig. 28- Simplified Schematic Diagram - Over-Voltage Protection Circuit for +5-Volt Supply

4. MAINTENANCE

(A) Required Test Equipment

4.01 The equipment listed in Table IV is required for maintenance of the Pattern Generator. The Common Name column of the table gives the names by which the test equipment will be called in the following maintenance procedures.

TABLE IV

REQUIRED TEST EQUIPMENT

NAME	COMMON NAME	FUNCTION
Electronic Frequency Counter, Hewlett-Packard Model H-P, or equivalent	Counter	Measurement of time-base frequencies and data rates.
Oscilloscope, Tetronix Model 535A, or equivalent	Oscilloscope	Waveform observation and measurement. Used also for signal tracing.
Multimeter, Simpson Model 260, or equivalent	Multimeter	General voltage and resistance measurements.

TABLE IV (Cont' d)

NAME	COMMON NAME	FUNCTION
Data Measuring Set, STELMA Model DMS-303A, or equivalent	DMS-303A	Measurement of telegraph distortion.
Teletype Printer Units (2 required: 5-level code and 8-level code machines)	Teleprinter	Provide printed read-outs of Pattern Generator output signals for verification of equipment accuracy.

(B) Performance Tests

4.02 A thorough performance test of the Pattern Generator requires that the various functional sections of the unit be tested and evaluated separately, since there is no one combination of control settings and associated measuring equipment that will provide a comprehensive test of the entire unit. Therefore, the performance testing outlined below is designed to cover the total unit in a logical series of separate tests. (See Fig. 29 through 57 at the end of this section for schematic, component location, and wiring diagrams.) The order of testing is as follows:

(a) Bit rates.

(b) Patterns, excluding selected character and random.

Note: These tests will also verify the performance of the high-level and low-level output circuits.

(c) Selected character patterns and code level modes.

(d) Distortion.

(e) External stepping.

(f) Random pattern.

Bit-Rate Tests

4.03 Preset Pattern Generator controls as follows:

(a) BIT RATE range selector to Range A.

(b) DISTORTION switches to zero and OFF.

(c) MODE switches to FREE RUN and SYNC.

(d) PATTERN switch to REV.

4.04 Proceed as follows:

(a) Using a frequency counter connected to the LOW LEVEL output terminals of the Pattern Generator, measure the output frequency at each numbered setting of the BIT RATE frequency selector (outer knob) . The frequency in bits per second indicated by the counter should correspond to one-half the bit-rate marking at each setting of the selector switch.

(b) Set BIT RATE frequency selector to the EXT position. Connect an external timing source having appropriate characteristics (see to Table I) to the EXT CLK connector at the rear of the unit. The output bit-rate indicated on the counter should be 1/200th of the input timing frequency.

(c) If the six optional crystals have been installed for range B, set the BIT RATE range selector to range B and repeat step (a) above for the first six positions of the BIT RATE frequency selector switch.

Output Circuits and Pattern Tests

4.05 The following tests verify the performance of the Pattern Generator at all settings of the PATTERN switch. Output signals are taken from both the high-level and low-level output terminals, thus completely testing the output circuits.

Steady Mark Steady Space, and Reversals

4.06 Preset Pattern Generator controls as follows:

(a) BIT RATE switch to Range A at 75 bits per second.

(b) DISTORTION switches to zero and OFF.

(c) MODE switches to FREE RUN and SYNC.

(d) PATTERN switch to STEADY, M.

4.07 Proceed as follows:

(a) (a) Turn on power and observe that SIG indicator lamp lights steadily (indicating steady Mark signal).

(b) Using voltmeter or dc oscilloscope, measure output at LOW LEVEL terminals. Output should be a steady +6 volts if Pattern Generator has been strapped for positive Mark (low-level). If strapped for negative Mark, output should be -6 volts. (See. 1.24 for strapping information.)

(c) Set PATTERN switch to STEADY, S. The SIG indicator lamp should go out, and the steady Space output voltage at the LOW LEVEL terminals should measure -6 volts if the unit is strapped for positive Mark, or +6 volts if strapped for negative Mark.

(d) Set PATTERN switch to REV and use an oscilloscope to verify presence of reversals signal at LOW LEVEL output terminals. The displayed signal should be a square-wave pattern having a peak-to-peak amplitude of 12 volts (-6 to +6 volts) at a rate of 75 bits per second.

FOX Message (5-level and 8-level)

4.08 Preset Pattern Generator controls as follows:

(a) BIT RATE switches to Range A at 75 bits per second.

(b) DISTORTION switches to zero and OFF.

(c) MODE switches to FREE RUN and START/STOP, 1.0.

(d) PATTERN switch to FOX MSG , 5.

4.09 Proceed as follows:

(a) Connect an appropriate 5-level teleprinter unit to the high-level output terminals. Be sure that the output loop circuit connection (polar or neutral) matches the input requirements of the teleprinter unit. (See 1.21 through 1.23 for information on external connections.)

(b) Set front-panel HI-LEVEL SELECT switch to POLAR or NEUT, in accordance with the connections made in step (a) above.

(c) Program the SELECTED CHARACTERS switches for any desired combination of characters. Depress the correspondingly numbered CHARACTER SEQUENCE LENGTH switch. (See Fig. 15 for 5-level code patterns.)

(d) Turn on power to units and observe that the FOX message format, including the six programed characters, is repeatedly generated and printed.

(e) For 8-level FOX message, repeat the above procedure using an appropriate 8-level teleprinter unit connected to the high-level output of the Pattern Generator. (See Fig. 16 for 8-level code patterns when programing the SELECTED CHARACTERS switches.

Selected Characters (5-Level and 8-Level)

4.10 The performance test for the 5-level and 8-level selected character patterns is essentially identical to the FOX message tests in 4.08 above. Preset the Pattern Generator the same way except for the PATTERN switch, which is set to CODE LEVEL 5 and CODE LEVEL 8 for the respective tests. Repeat the procedure of paragraph 4.09. The CHARACTER SEQUENCE LENGTH selection function should be tested by depressing the six numbered buttons sequentially and observing that the corresponding number of the six programed characters is repeatedly generated and printed.

Selected Characters (6-Level and 7-Level)

4.11 To verify the performance of the Pattern Generator in the 6-level and 7-level selected character positions of the PATTERN switch, the output pattern must be viewed on an oscilloscope. Preset the Pattern Generator controls as follows:

(a) BIT RATE switches to Range A at 75 bits per second.

b) DISTORTION switches to zero and OFF.

(c) MODE switches to W STEP, CHAR and START/STOP, 1.0 UNIT STOP MARK.

(d) PATTERN switch to SELECTED CHARACTERS, CODE LEVEL 6.

(e) SELECTED CHARACTERS switches -- Program a Mark into all six bit positions of all six characters. (Depress all switches.)

(f) CHARACTER SEQUENCE LENGTH switches -- Depress number 6.

4.12 Proceed as follows:

(a) Connect oscilloscope vertical input to LOW LEVEL output terminals of Pattern Generator.

(b) Connect external sweep trigger input of oscilloscope to TP7 of PC-card A7 (accessible at rear of unit). Set scope for external, positive sync.

(c) Turn on equipment and step characters manually, using RELEASE pushbutton. Each character displayed should show a full complement of Marks in the bit pattern.

(d) Release all odd numbered switches, thus restoring them to Space condition, and repeat step (c) above. Displayed patterns should indicate alternate Mark/Space bit pattern having Marks in second, fourth, and sixth positions.

(e) Release all remaining switches and repeat step (c). Each displayed character should contain a full complement of Spaces in each bit position.

(f) Set PATTERN SWITCH to the 7 position of SELECTED CHARACTERS, and repeat above procedures for 7-level code.

Distortion

4.13 Distortion testing requires the use of a data measuring set (such as the STELMA DMS-303A Analyzer) having distortion-measuring capabilities commensurate with the Pattern Generator specifications. The indicated distortion settings of the Pattern Generator front-panel controls are verified and measured by the data measuring set. Pre - set the Pattern Generator controls as follows:

(a) BIT RATE switches to Range A at 75 bits per second.

(b) PATTERN switch to SELECTED CHARACTERS, CODE LEVEL 5.

(c) MODE switches to FREE RUN and START/STOP, 1.0 UNIT STOP MARK.

4.14 Proceed as follows:

(a) Connect the DMS-303A Analyzer to the LOW LEVEL output terminals of the Pattern Generator.

(b) Set the DISTORTION - TYPE switch of the Pattern Generator to BIAS, M. Adjust the controls of the DMS-303A for measurement of Marking bias on a low-level start-stop signal.

(c) Program the SELECTED CHARACTERS switches for character no. 1 to provide alternate Marks and Spaces. Depress CHARACTER SEQUENCE LENGTH switch no. 1.

(d) Set both DISTORTION - PERCENT switches to O (zero) positions.

(e) Turn on equipment and observe distortion indication on meter of DMS-303A. Distortion should be zero.

(f) Set the decade (small inner) knob of the Pattern Generator DISTORTION - PERCENT switches to the 10 position. The DMS-303A meter should now indicate distortion of 10 per cent ±2 per cent.

(g) Set decade knob to remaining three positions (20, 30, and 40 per cent positions). At each step, the DMS-303A meter should indicate the corresponding amounts of distortion present on the output signal, ±2 per cent.

(h) Set the decade DISTORTION - PERCENT switch to 0 (zero). The DMS-303A should indicate zero distortion again.

(i) Set the units (large outer) knob of the DISTORTION - PERCENT switch sequentially to each numbered position (up to 9). At each numbered position the corresponding amount of distortion should be indicated on the DMS-303A meter, ±2. per cent.

(j) Set the decade knob to 20 and repeat step (i) above. The distortion indication on the DMS-303A meter should now be the sum of 20 plus the numbered units setting, ±2 per cent.

(k) Measure the output distortion for all remaining positions of the DISTORTION - TYPE switch (Spacing bias, switched bias, Marking end, and Spacing end). Use same general procedure as outlined above for Marking bias.

External Character Stepping

4.15 This function may be verified with the Pattern Generator setup for the 5- or 8-level Selected Characters test (see 4.10) or the FOX message test (paragraph 4.08). The procedure is as follows:

(a) Connect external stepping source signal wires between STEP IN and GND input terminals on rear-panel terminal board. (See Table I for electrical specifications of stepping signals.) (See 1.25 for information on applicable strapping.)

(b) Set MODE switch to EXTERNAL, CHAR STEP or EXTERNAL, SEQ STEP.

(c) Turn on equipment. Selected output program should now be generated in step with the externally applied signal.

Random Pattern Check

4.16 This test should be performed in conjunction with the associated DMS-303A Analyzer, since this feature of the Pattern Generator was designed to be compatible with the bit-error measuring capabilities of the DMS-303A. (The 511-bit random pattern output conforms to the standard established by CCITT.) Preset the Pattern Generator controls as follows:

(a) PATTERN switch to RAND.

(b) DISTORTION switches to zero and OFF.

(c) BIT RATE switches to same rate as DMS-303A.

(d) MODE switches to FREE RUN and SYNC.

4.17 Set the DMS-303A controls in accordance with the instructions contained in the applicable manual. Connect the LOW LEVEL output of the Pattern Generator to the INPUT SIG jack of the DMS-303A. Turn on equipment and proceed as follows:

(a) Press the PUSH TO SYNC switch on the DMS-303A Analyzer.

(b) Reset the DMS-303A display circuits by actuating the DISPLAY RESET switch to the MAN position. The meter should indicate no bit errors, thereby verifying that the two units are synchronized.

(c) Troubleshooting and Fault Isolation

4.18 The information presented below is a suggested approach to analyzing trouble symptoms and isolating faults down to the assembly or circuit level. This approach is most valuable if performed in conjunction with a performance test, because each part of these tests generally pertains to specific functional circuits or assemblies of the unit. A conventional troubleshooting table is not supplied because of the usual

limitations of this approach, i.e., the impracticality of making such a table comprehensive enough to cover all possible fault condition-s and resultant symptoms. Instead, it will be assumed that the technician or engineer has accumulated enough basic and detailed knowledge of this unit to permit him to analyze and locate troubles through reasoning, using suitable measuring test equipment. Finally, it is assumed that prior to undertaking trouble analysis the usual preliminary steps and measures have been taken; these measures include visual inspection of the equipment to uncover faults such as loose or broken assemblies, connectors, wiring, etc., and a check of the primary input power and power supply voltages.

4.19 The power supply fuses and the power supply voltages should be checked before disassembling the unit for further testing. Three of the fuses are mounted on power supply PC-card A2. In addition, fuses are located in each leg of the battery inputs of the high-level loop output circuit. If the equipment malfunction has occurred during high-level output operation, these fuses (located on PC-card A3) should be among the first things to check. To remove the power supply card, the two knurled, captive, securing screws at the top must first be loosened. The procedure for checking the power supply output voltages is covered in (E) Power Supply Adjustment Procedures. If power supply voltages are normal, signal tracing and waveform observation, using an oscilloscope, must be performed on the signal portions of the unit.

4.20 Trouble analysis of the Pattern Generator must proceed in a logical order to isolate the cause of faults by “process of elimination.” The different functional sections and assemblies of the unit, as described in the Principles of Operation portion of this manual, must be thought of both in terms of their individual characteristics and in terms of how they interact and are, in numerous cases, mutually interdependent. Thus, certain malfunctions may render the whole unit inoperative, whereas other malfunctions may cause only one or more output patterns to be adversely affected. As a guide for signal tracing and trouble analysis, a selected sampling of waveform data is provided in the subsequent paragraphs. The information presented is intended to serve as a starting point for checking the functioning of the various assemblies and circuits. The data represents the “norm” for a given set of conditions. The following items merit emphasis:

(a) The waveforms were taken at the numbered test point terminals on the PC-cards. For each waveform, a particular set of operating control settings of the Pattern Generator is used; these control settings are specified and should be duplicated when signal tracing with the oscilloscope.

(b) When signal tracing, it is suggested that the applicable PC-card schematic diagrams be referred to frequently. Use of schematic diagrams will facilitate signal tracing on a point-to-point basis when using test points other than the established numbered terminals. Such procedures will usually be needed to locate defective circuit parts (such as I-C modules) and require a thorough understanding of the many individual circuits that constitute the unit.

4.21 Assembly A1: Unless otherwise indicated, waveform measurements are obtained using the following Patterm Generator control settings:

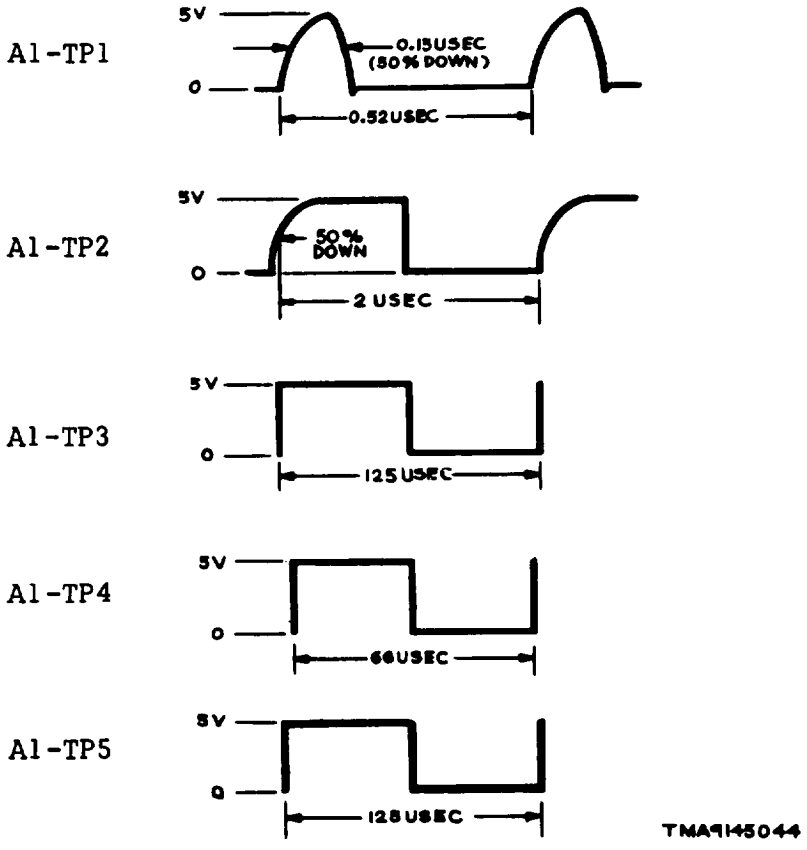
PATTERN . . . . . REV

MODE . . . . . FREE RUN, SYNC

DISTORTION . . . . . zero, OFF

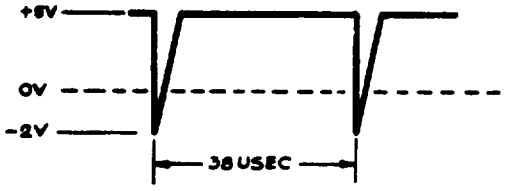
BIT RATE 75

Oscilloscope set for triggered sweep; triggering source: A7-TP7

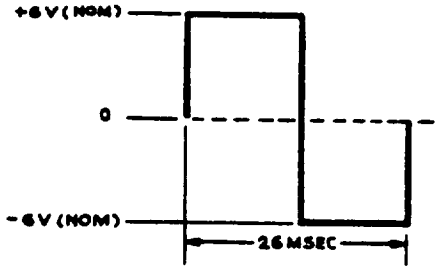


4.22 Assembly A3: Control settings and oscilloscope settings same as for Assembly A1, unless otherwise noted.

A3-TP1
(PATTERN switch set to STEADY Space.)



A3-TP3



TMA9145045

4.23 Assembly A4: Unless otherwise indicated, waveform measurements are obtained with the Pattern Generator controls set as follows:

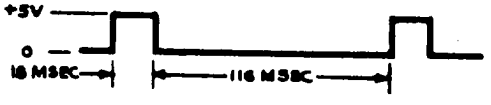
PATTERN ..... FOX MSG-5

MODE ..... FREE RUN, START/STOP, 1.0

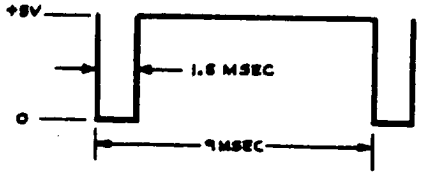
DISTORTION ..... zero, OFF

BIT RATE 4800

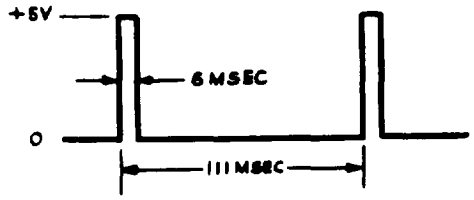
A4-TP3



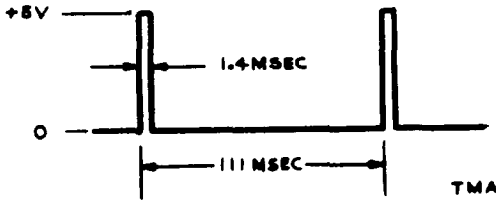
A4-TP4
(PATTERN switch set to SELECTED CHARACTERS -5; CHARACTER SEQUENCY LENGTH switch number 5 depressed.)



A4-TP5
(PATTERN switch set to FOX MSG-8.)

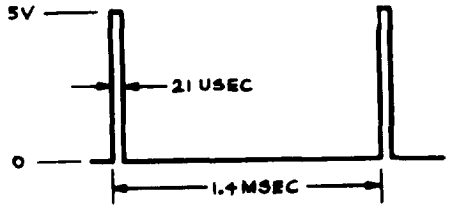


A4-TP6

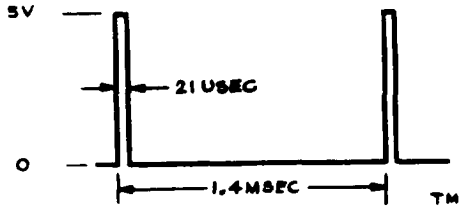


TMA9145046

A4-TP7
(PATTERN switch set to SELECTED CHARACTERS -5.)



A4-TP8
(Same settings as for A4-TP7.)



TMA9145047

4.24 Assembly AS: Unless otherwise indicated, waveform measurements are obtained with the Pattern Generator controls set as follows:

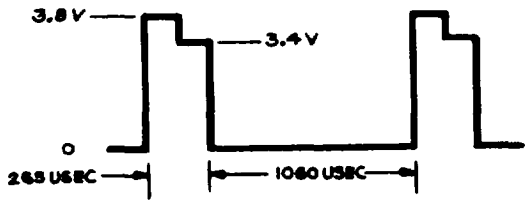
PATTERN ..... REV

MODE ..... FREE RUN, SYNC

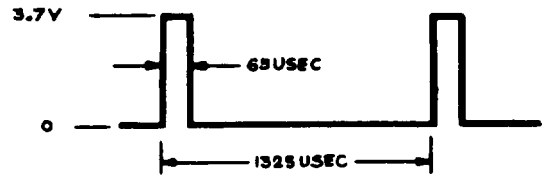
DISTORTION ..... zero, OFF

BIT RATE 75

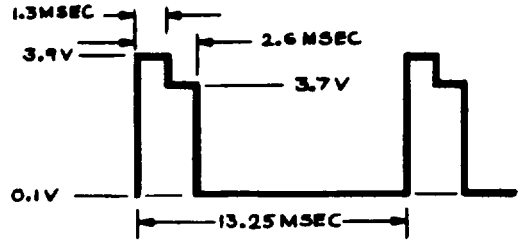
A5-TP1



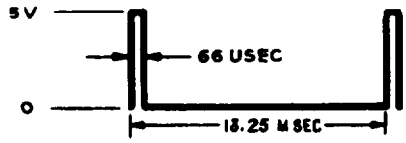
A5-TP2



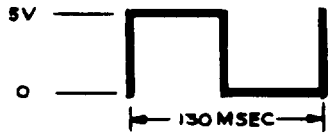
A5-TP3



A5-TP4



A5-TP5
(PATTERN switch set to SELECTED CHARACTERS -5; DISTORTION/TYPE switch set to SW BIAS.)



TMA9145048

4.25 Assembly A6: Unless otherwise indicated, waveform measurements are obtained with the Pattern Generator controls set as follows:

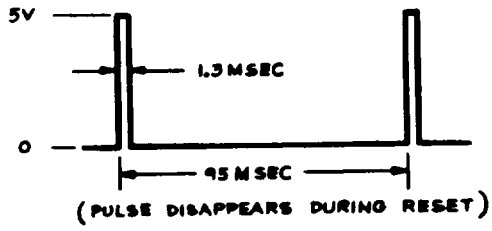
PATTERN..... FOX MSG -5

MODE..... FREE RUN, START/STOP, 1.0

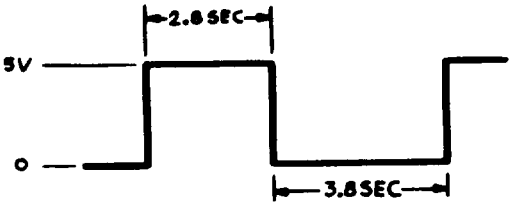
DISTORTION ..... zero, OFF

BIT RATE..... 75

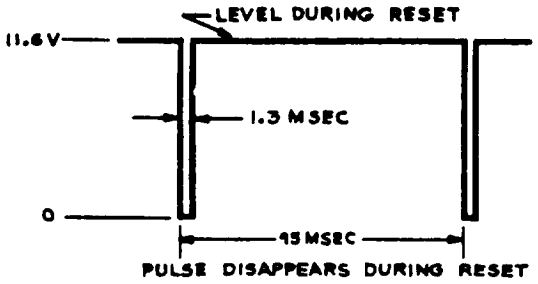
A6-TP1



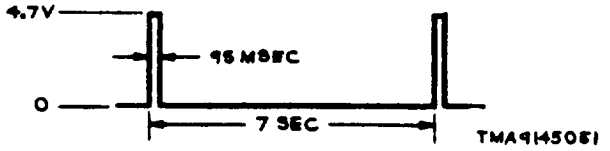
A6-TP2



A6-TP3



A6-TP4



4.26 Assembly A7: Unless otherwise indicated, waveform measurements are obtained with the Pattern Generator controls *set* as follows:

PATTERN ..... SELECTED CHARACTERS -8

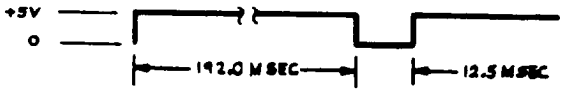
DISTORTION ..... zero, OFF

MODE ..... FREE RUN, START/STOP, 1.0

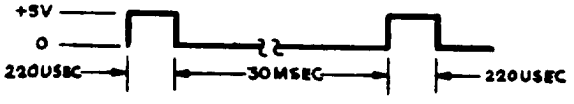
BIT RATE 600

(Any 8-bit pattern should be programed into the SELECTED CHARACTERS switch matrix.)

A7-TP1

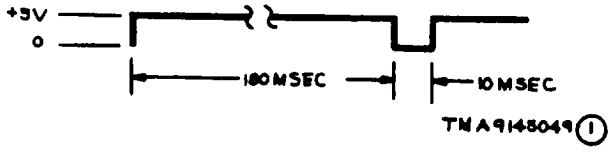


A7-TP2

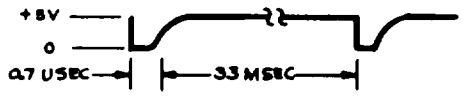


A7-TP3
(PATTERN switch set to REV.)

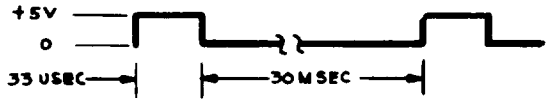
A7-TP4
(Same as for TP1, except MODE switch set to MAN STEP/CHAR rather than FREE RUN.)



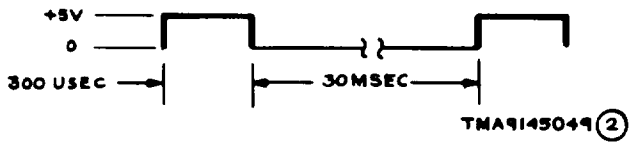
A7-TP5
(Same as for TP1, except MODE switch set for 1.5 unit Stop-Mark.)



A7-TP6



A7-TP7



4.27 Assembly A8: Unless otherwise indicated, waveform measurements are obtained with the Pattern Generator controls set as follows:

PATTERN ..... SELECTED CHARACTERS -8

MODE ..... FREE RUN, SYNC

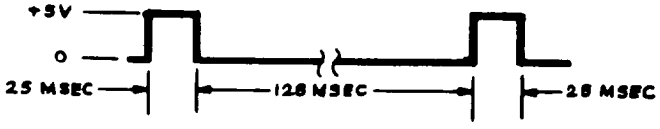
DISTORTION ..... zero, OFF

BIT RATE 300

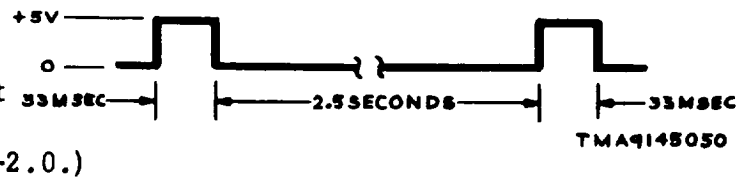
CHARACTER SEQUENCE
LENGTH switches ..... Depress No. 1.

Program all 8 bits of character No. 1 of the SELECTED CHARACTERS switch matrix as Marks (depress all switches).

A8-TP1 through A8-TP8



A8-TP9
(Same as for A8-TP1, except PATTERN switch set to FOX MSG-8 and MODE switch set to START/STOP-2.0.)



(D) Repairs

4.28 Repairs and replacement of Pattern Generator components may be accomplished using standard techniques and practices, including the precautionary measures required when replacing transistors and integrated circuits. In most cases, component replacement will not necessitate recalibration or readjustment of the unit, assuming an exact replacement part has been used. However, if any parts are replaced in the power supply circuits of PC-card A2, the applicable adjustment procedures for these circuits should be performed to restore these circuits to their factory-adjusted status.

(E) Power SUPPLY Adjustment Procedures

4.29 Procedures are given below for the adjustment of power supply output voltages. Because there is a degree of interdependence and interaction between the power supply circuits, it is important that these adjustments be carried out in the order given.

Note: The -15-volt supply voltage level is established at the factory by selection of the appropriate resistance value for A2R15 after the +15-volt supply is adjusted. Therefore, whenever the +15-volt supply is subsequently adjusted, the -15-volt level should automatically be correct.

(a) +15-Volt Adjustment

(1) Remove rear cover from enclosure to expose PC-cards.

(2) Connect unit to ac line and turn on power.

(3) Connect negative lead of dc voltmeter to TP3 (ground) of PC-card A2; connect positive lead to TP1 of AZ.

(4) Adjust trim-pot R6 (see Fig. 4) for an indication of exactly 15.0 volts on the voltmeter.

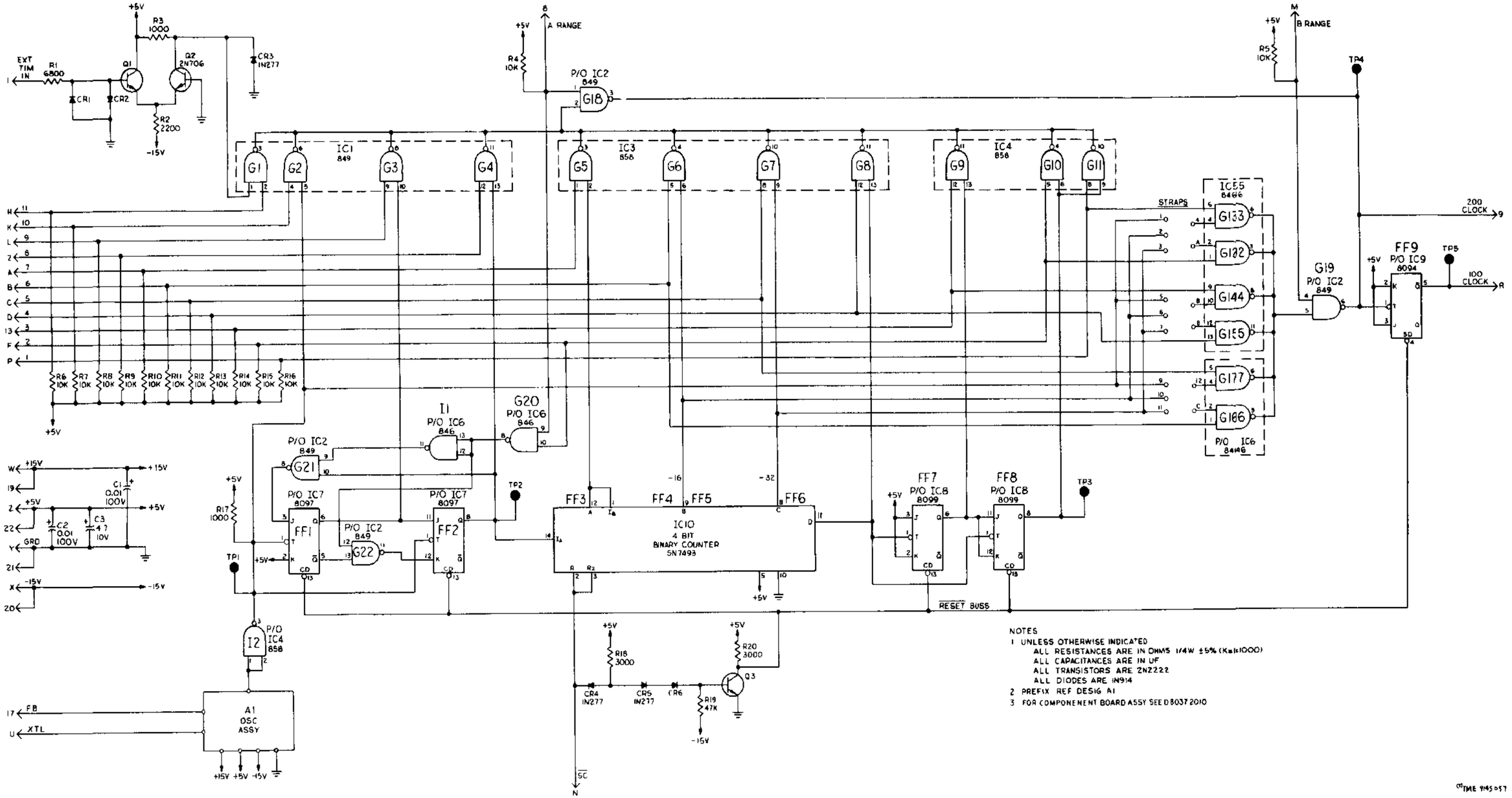
(5) Verify the presence and accuracy of -15-volt supply output. Connect negative lead of meter to TP4 on PC-card A2 and positive lead to TP3. Meter should indicate - 15-volt dc (±5 per cent).

(b) +5-Volt Adjustment

(1) Reconnect negative lead of voltmeter to TP3 and connect positive lead to TP2.

(2) Adjust trim-pot R21 (see Fig. 4) for an indication of exactly 5.0 volts on the voltmeter.

(3) Disconnect the voltmeter and replace the rear cover of the unit.



NOTES
1 UNLESS OTHERWISE INDICATED
ALL RESISTANCES ARE IN OHMS 1/4W ±5% (K=k1000)
ALL CAPACITANCES ARE IN UF
ALL TRANSISTORS ARE 2N2222
ALL DIODES ARE IN914
2 PREFIX REF DESIG A1
3 FOR COMPONENENT BOARD ASSY SEE D8037 2010

CT TIME 9145 057

Fig. 29 - Schematic Diagram - Time-Base Circuit, Assembly A1

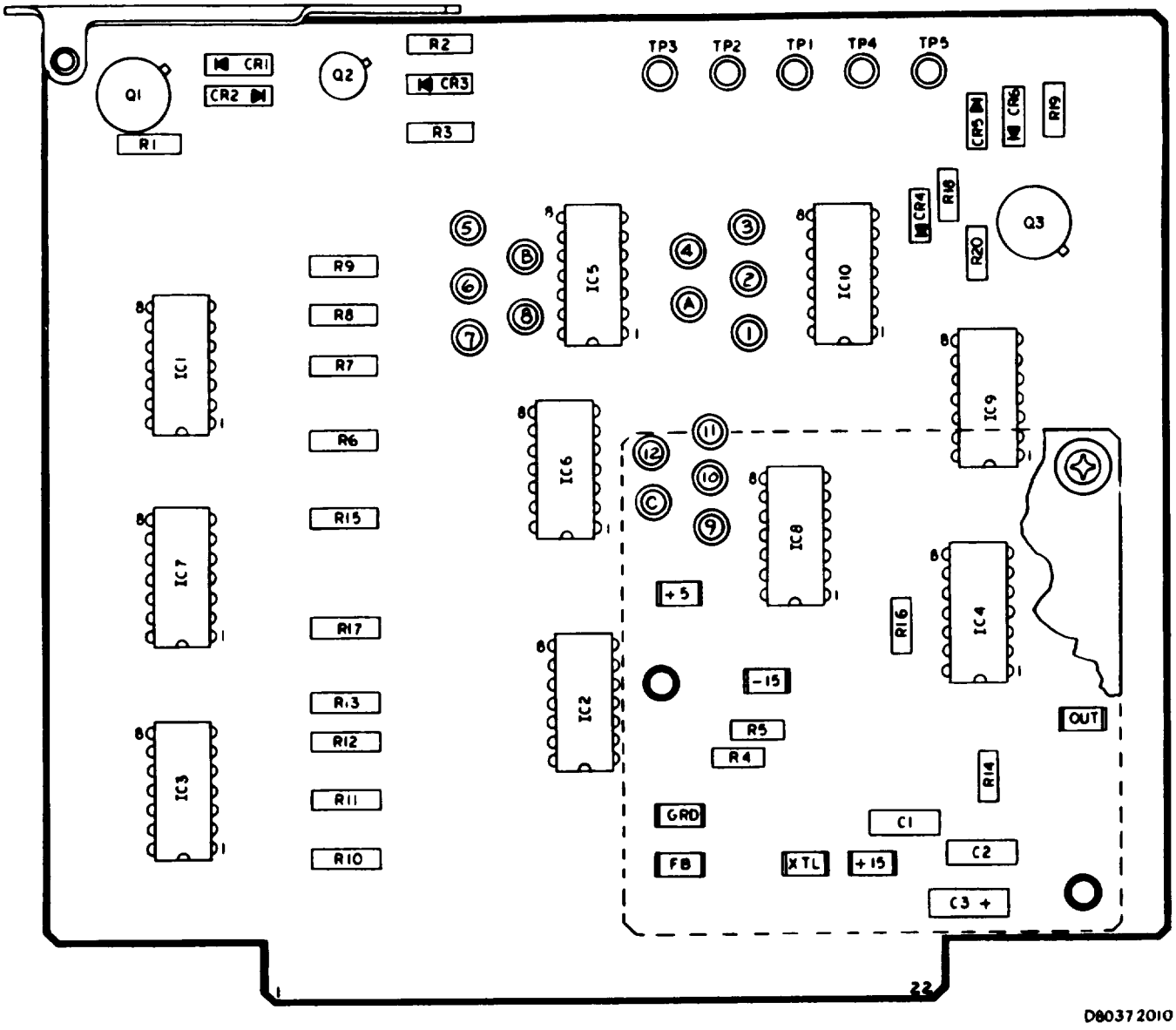
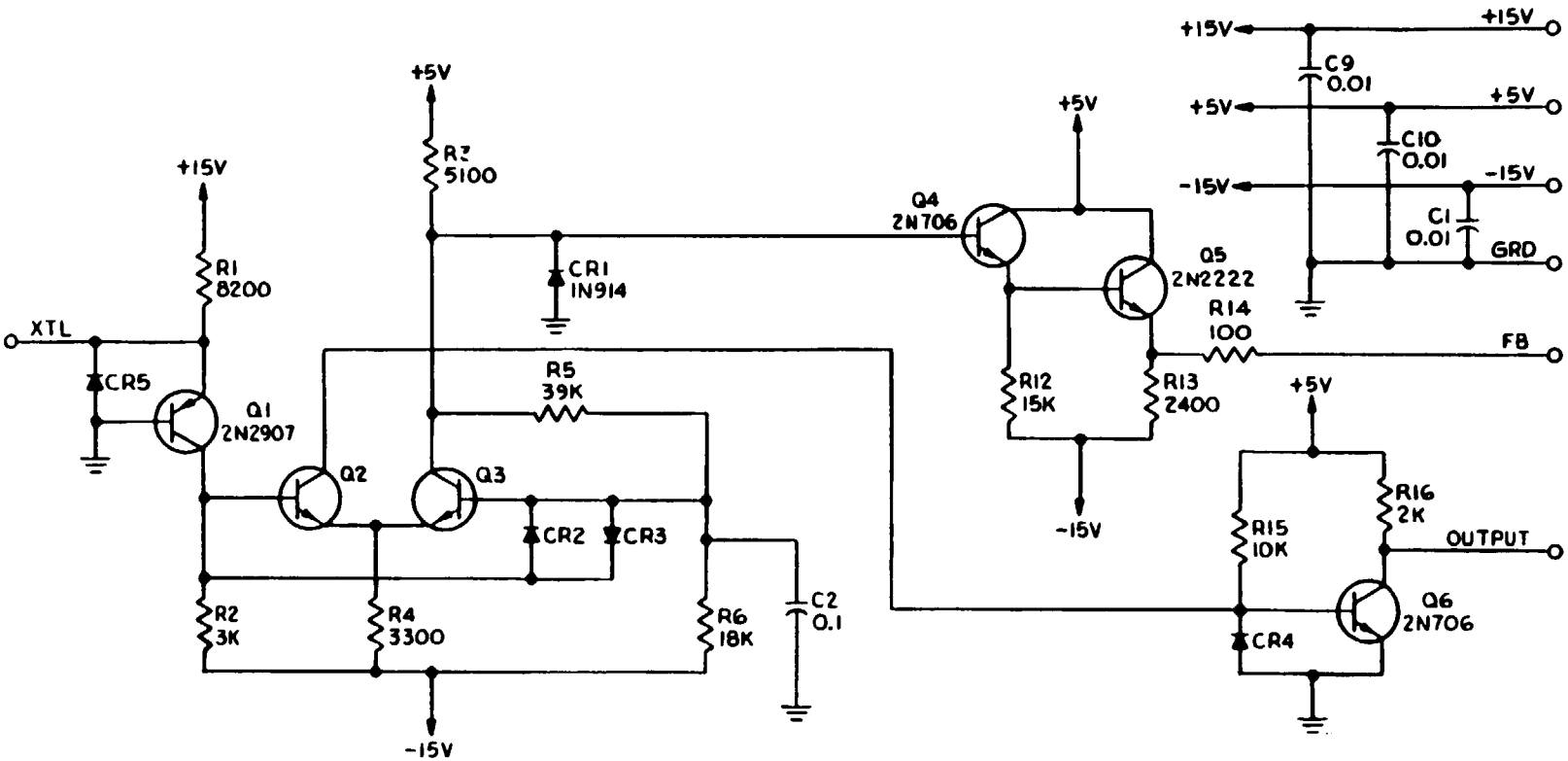


Fig. 30 Component Locations - Time-Base Circuit, Assembly A1



NOTES:

1. UNLESS OTHERWISE INDICATED,
   ALL RESISTANCES ARE IN OHMS,
   1/4W, ±5% (K=1000)
   ALL CAPACITANCES ARE IN UF.
   ALL TRANSISTORS ARE 2N5222.
   ALL DIODES ARE IN277.
2. PREFIX REF DESIG. A1A146

(1) TMC 9145 060

Fig. 31 - Schematic Diagram - Time-Base Oscillator, Subassembly A1A1

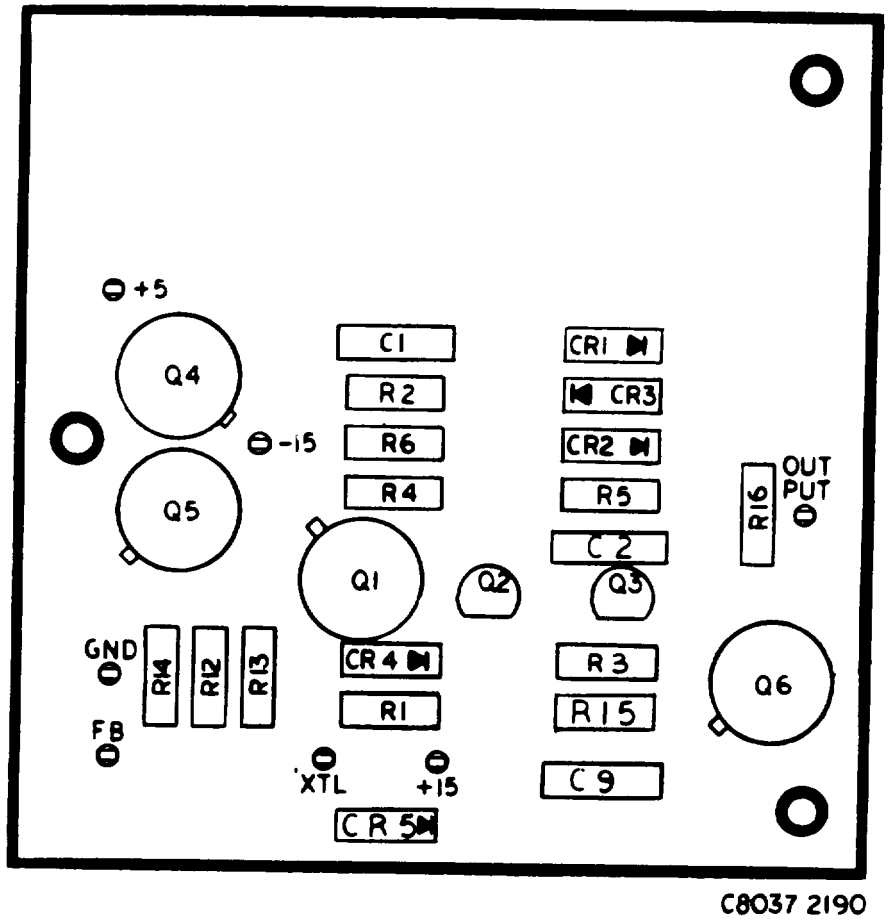


Fig. 32 - Component Locations - Time-Base Oscillator, Subassembly A1A1

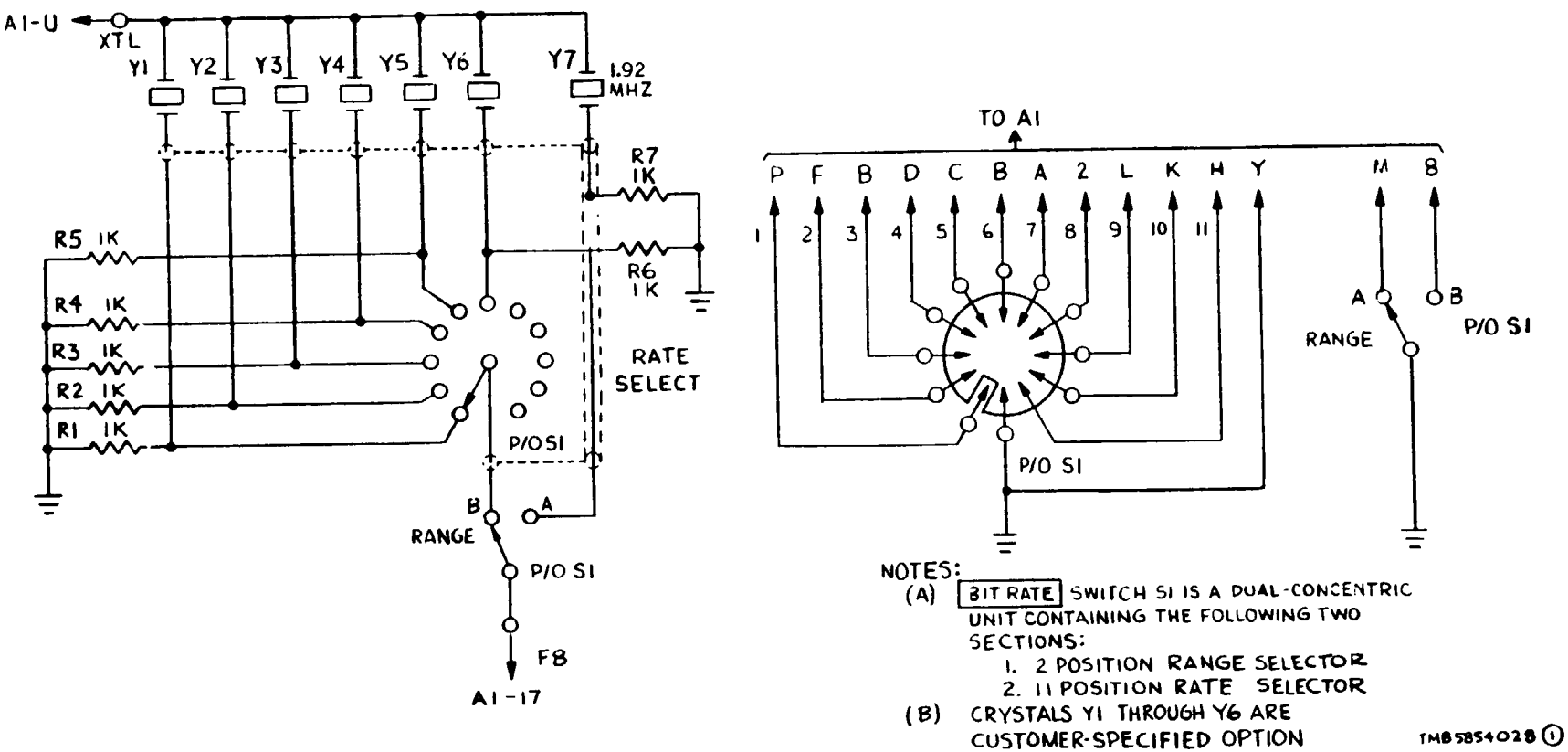
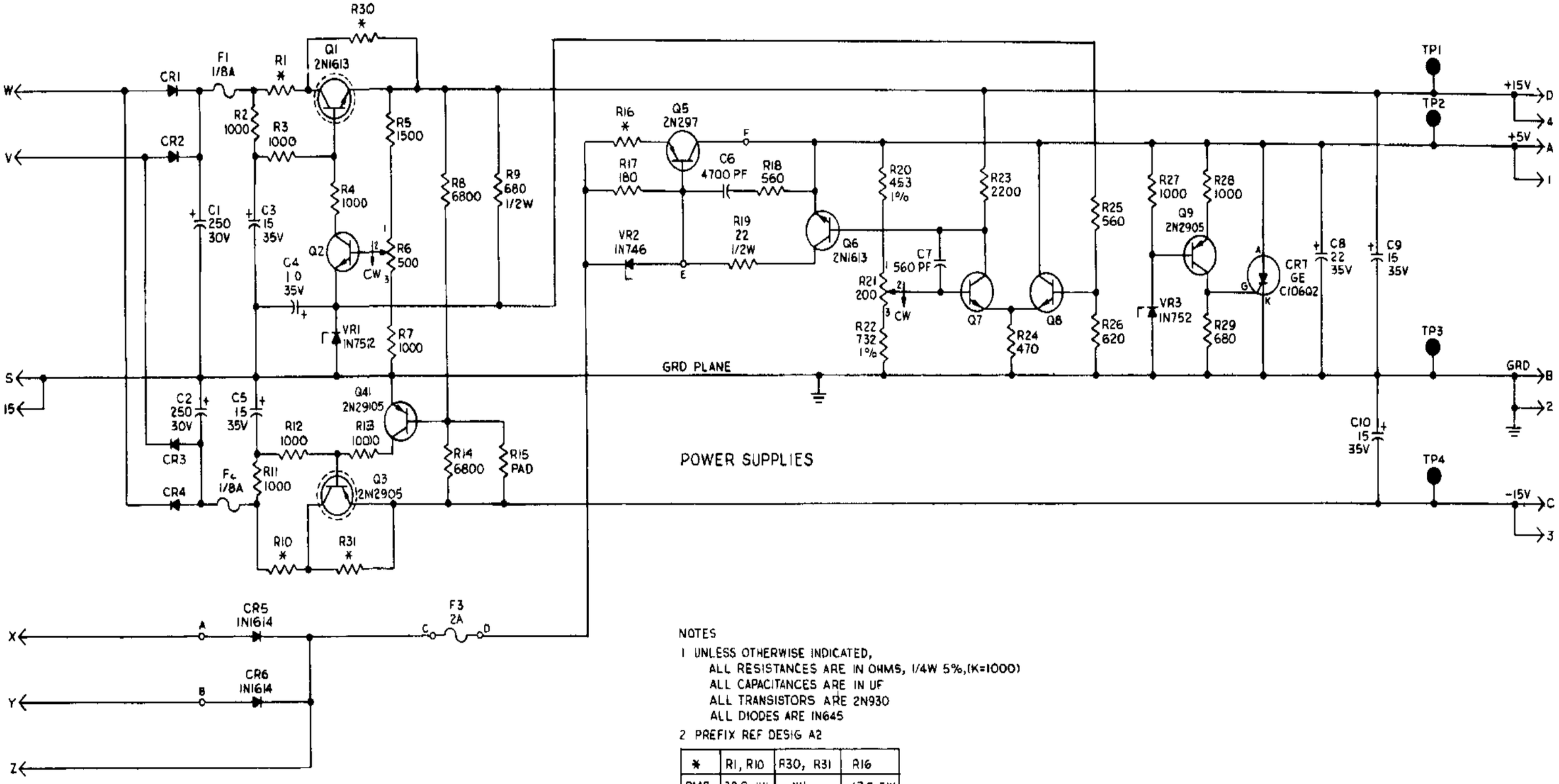


Fig. 33 - Schematic Diagram - Time-Base Crystal Bracket, Assembly A11



NOTES

1 UNLESS OTHERWISE INDICATED,
ALL RESISTANCES ARE IN OHMS, 1/4W 5%,(K=1000)
ALL CAPACITANCES ARE IN UF
ALL TRANSISTORS ARE 2N930
ALL DIODES ARE IN645

2 PREFIX REF DESIG A2

*	R1, R10	R30, R31	R16
DMS	39Ω 1W	NU	47Ω 5W
PG	22Ω 1W	180Ω,1/2W	1Ω, 5W

3 FOR COMPONENT BOARD ASSY SEE D80372020

TMD9145061

Fig. 34 - Schematic Diagram - Power Supply Circuits, Assembly A2

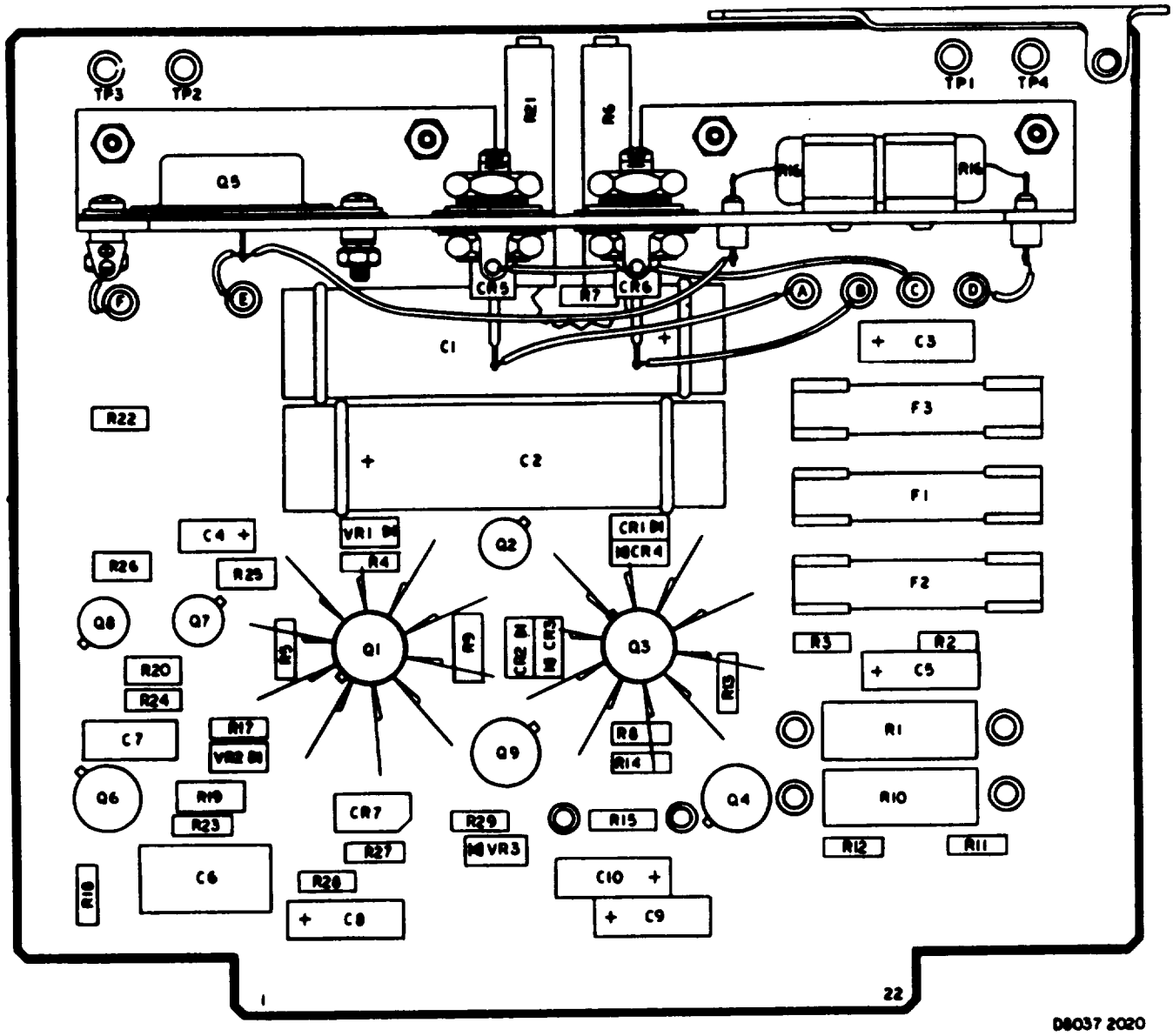


Fig. 35 - Component Locations - Power Supply Circuits, Assembly A2

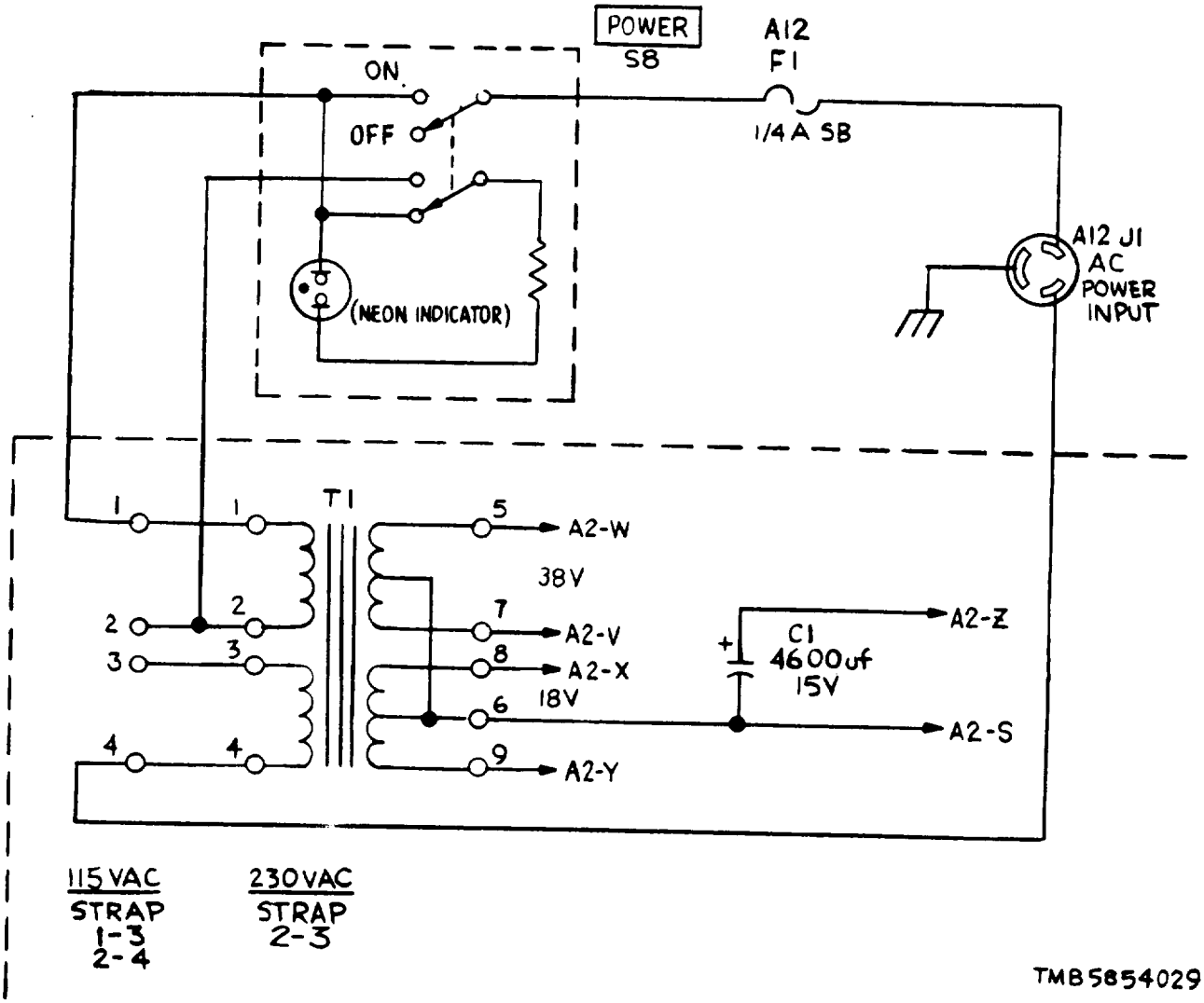


Fig. 36 - Schematic Diagram - Power Supply Primary Circuits, Assembly A12

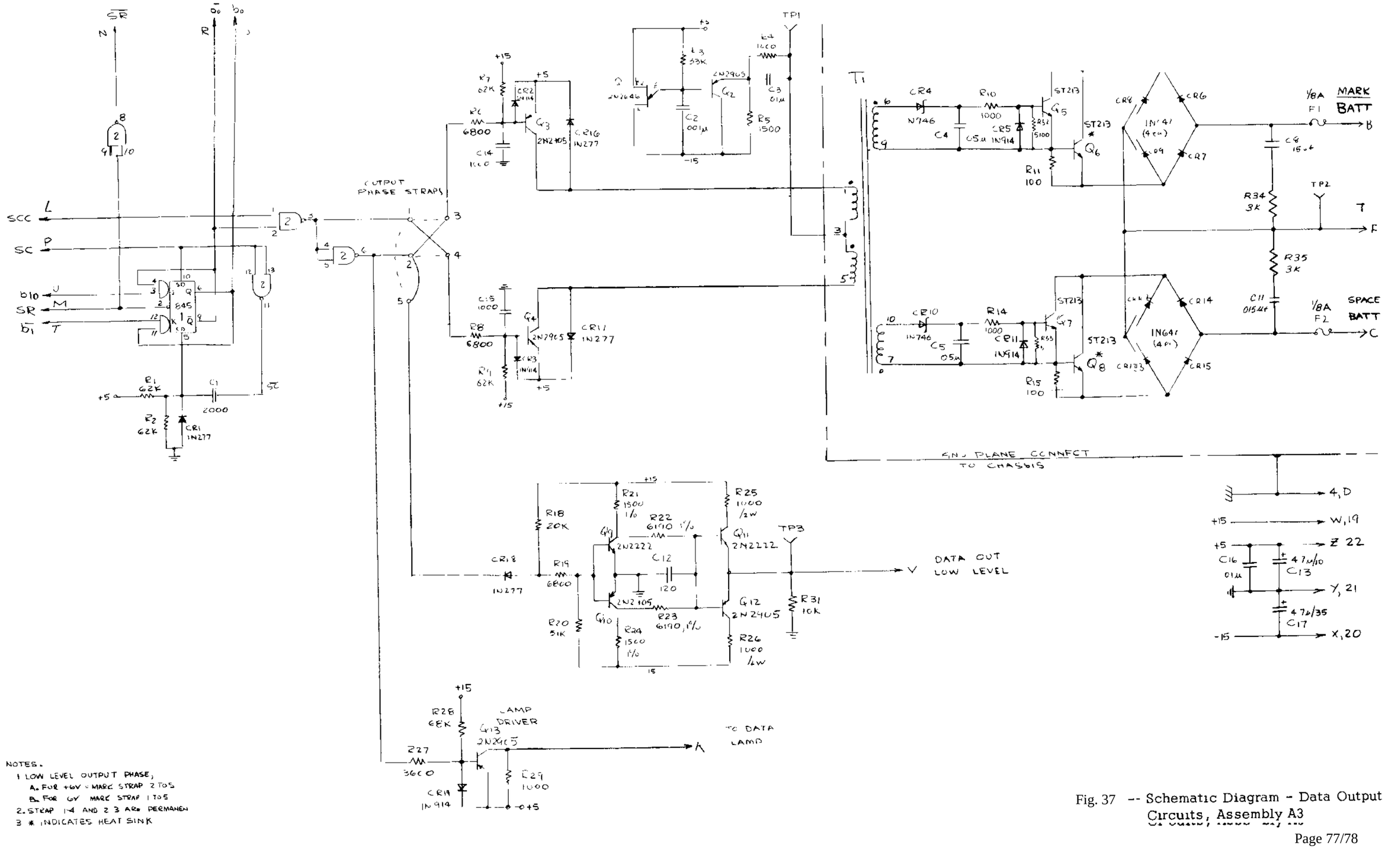


Fig. 37 -- Schematic Diagram - Data Output Circuits, Assembly A3

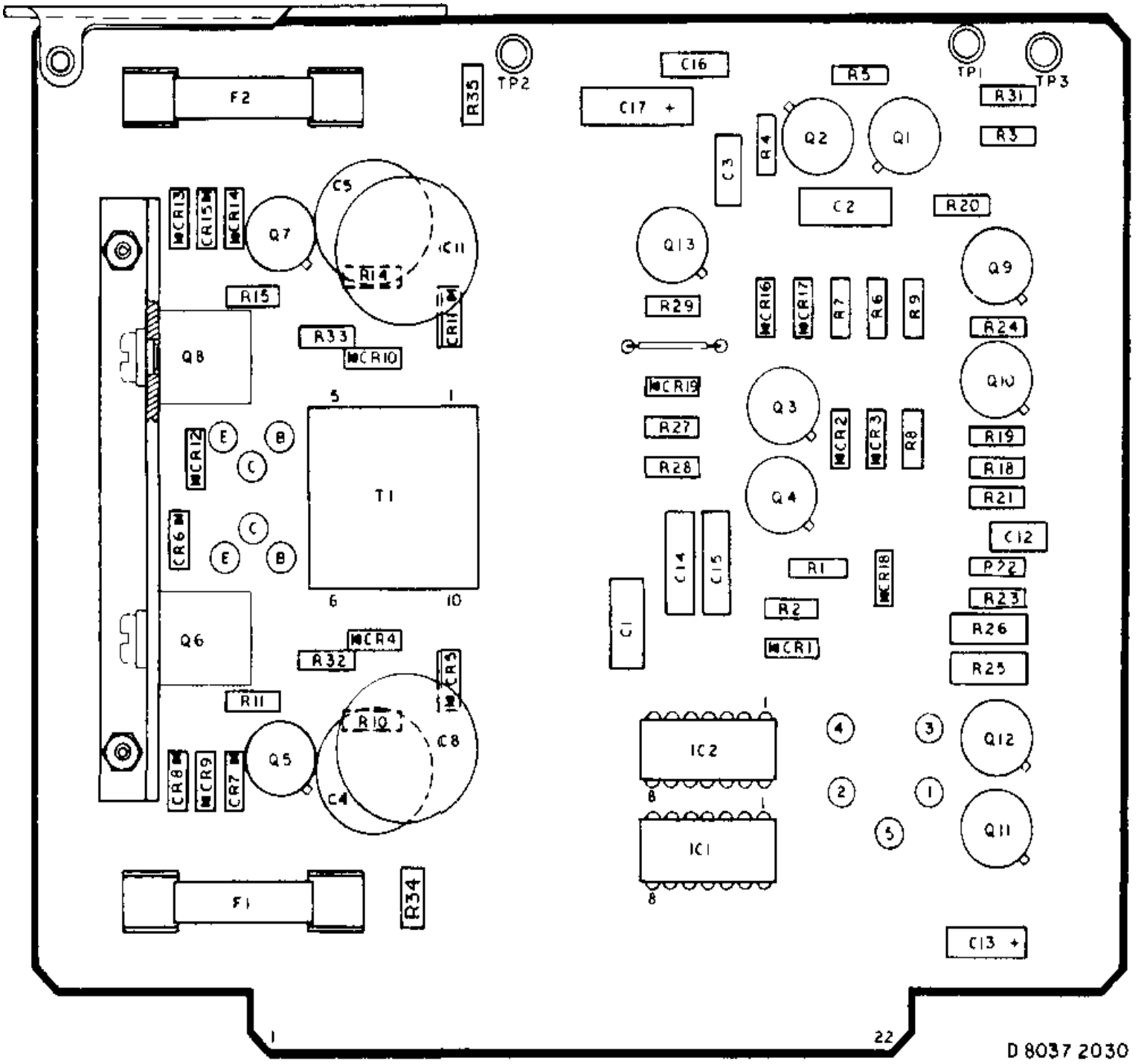


Fig. 38 - Component Locations - Data Output Circuits, Assembly A3

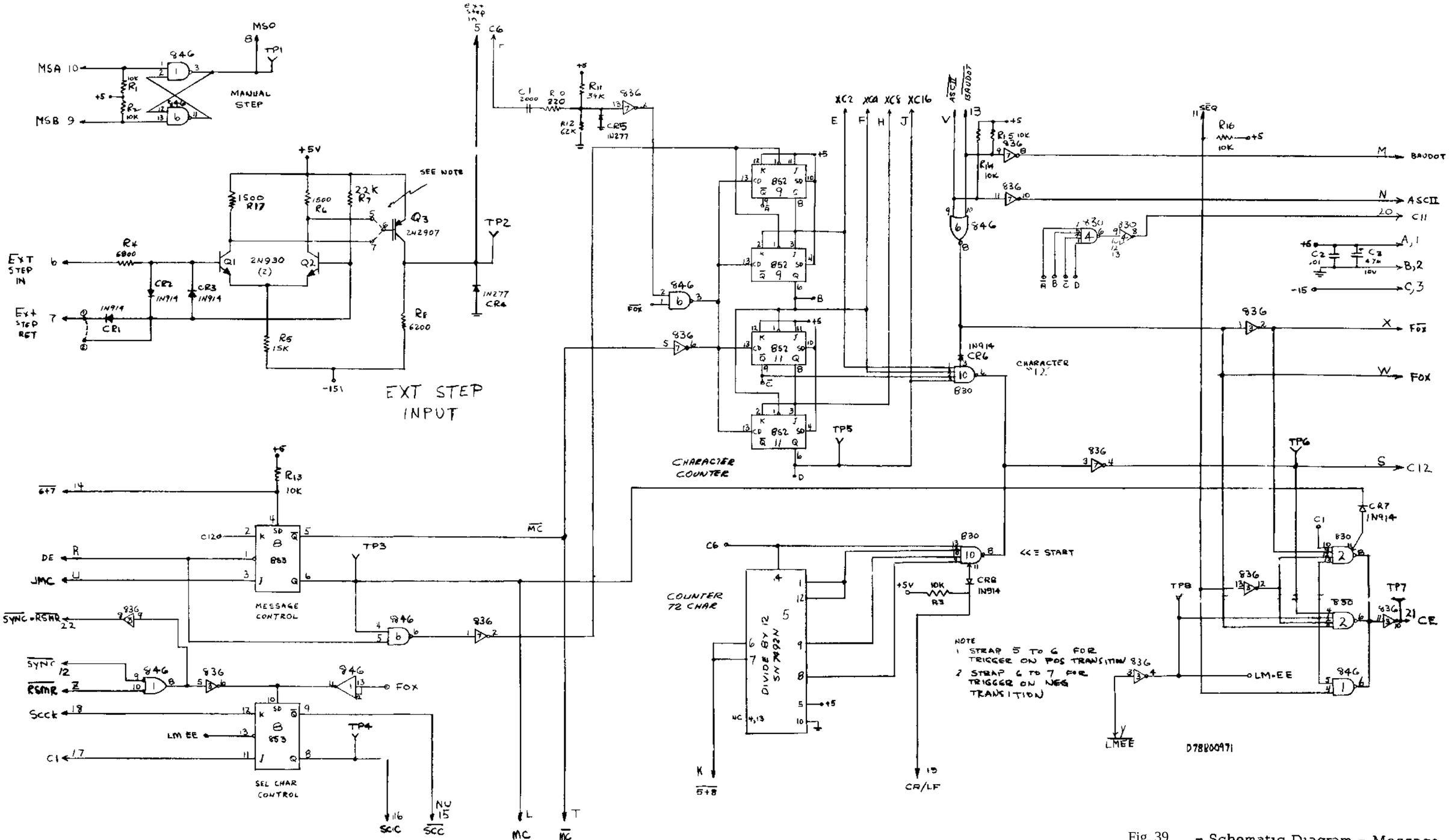


Fig. 39 - Schematic Diagram - Message Control Circuits, Assembly A4

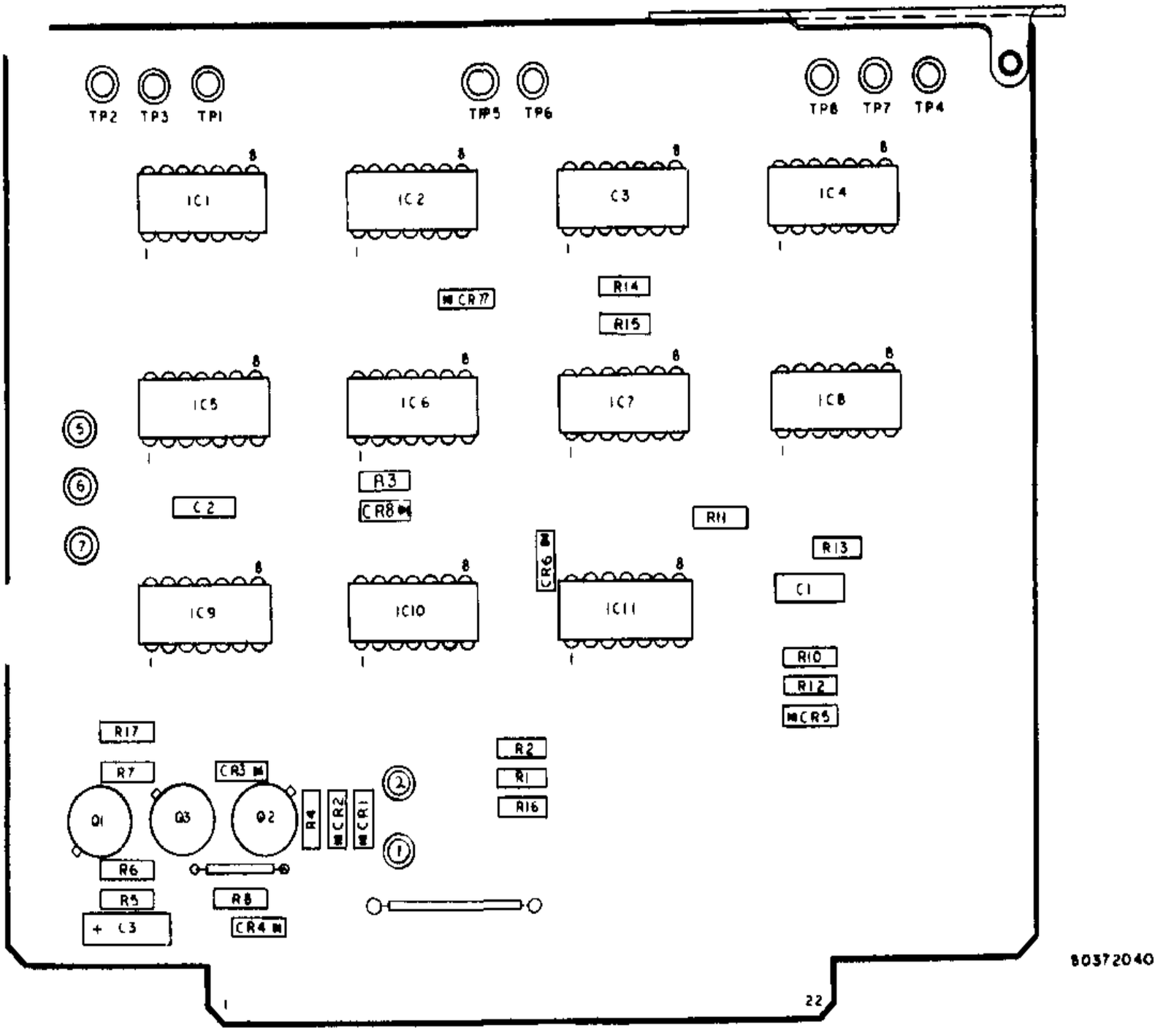
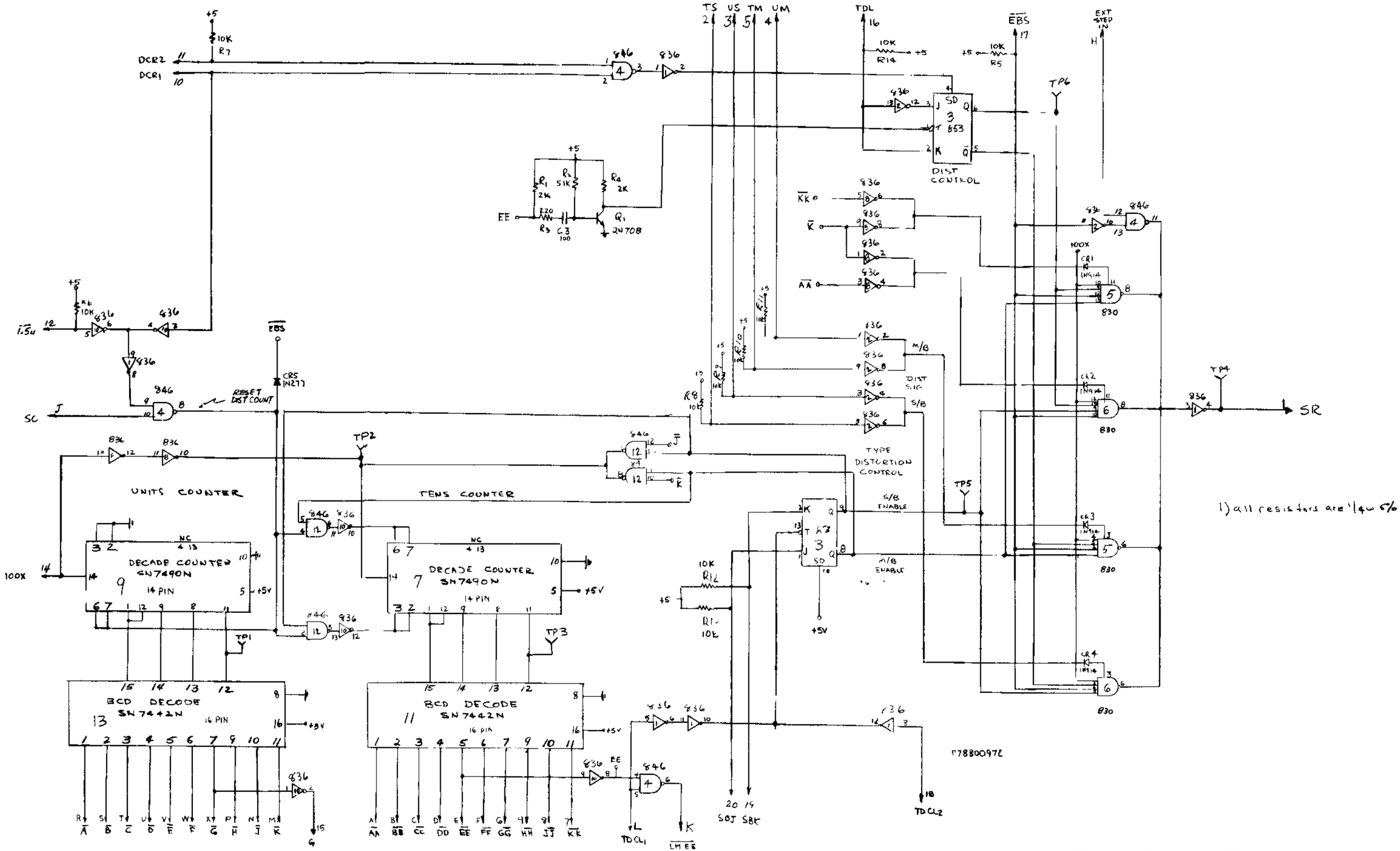


Fig. 40 - Component Locations - Message Control Circuits, Assembly A4



1) all resistors are 1/4w 5%

Fig. 41 - Schematic Diagram - Distortion Generator Circuits, Assembly A5

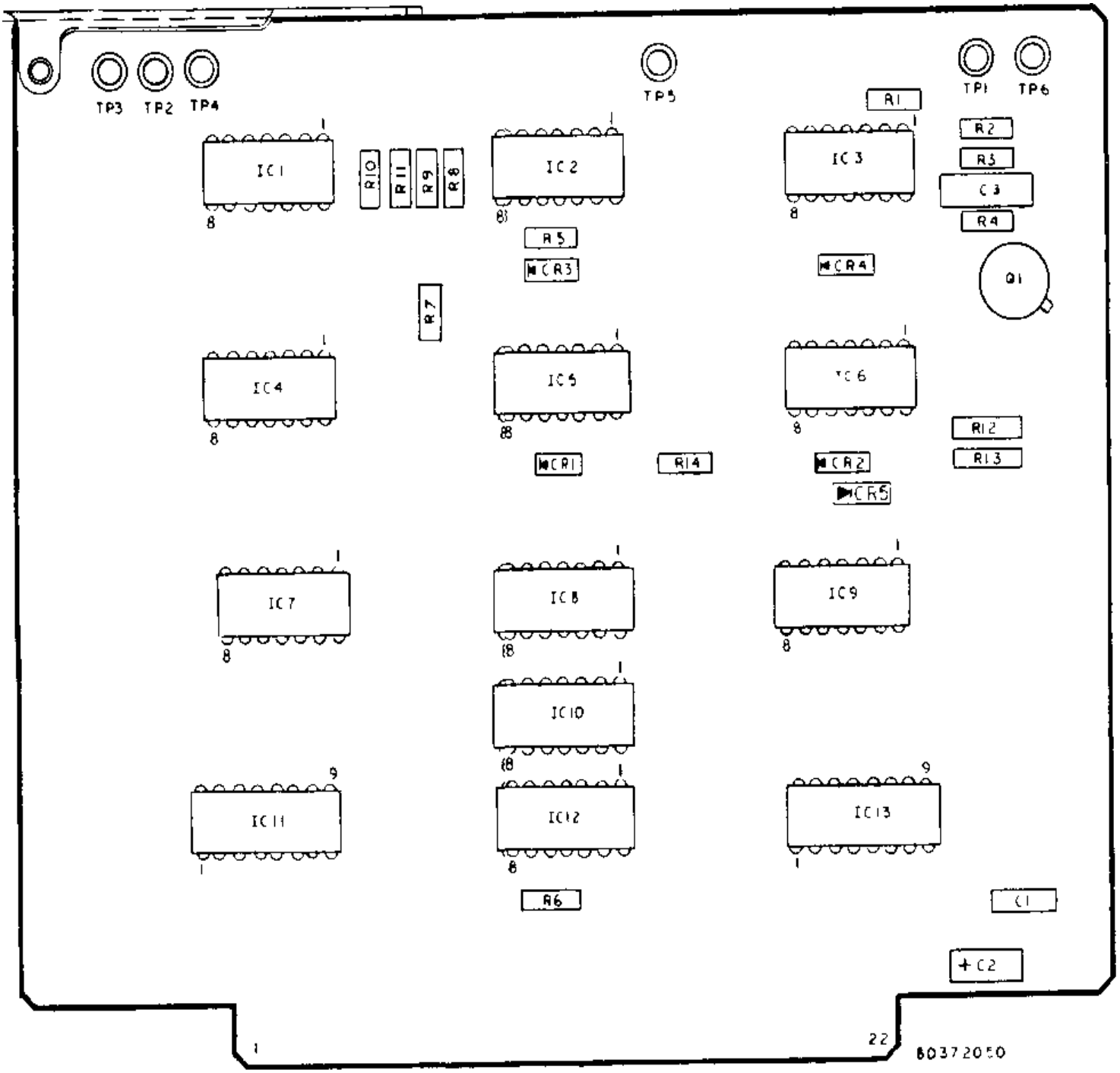
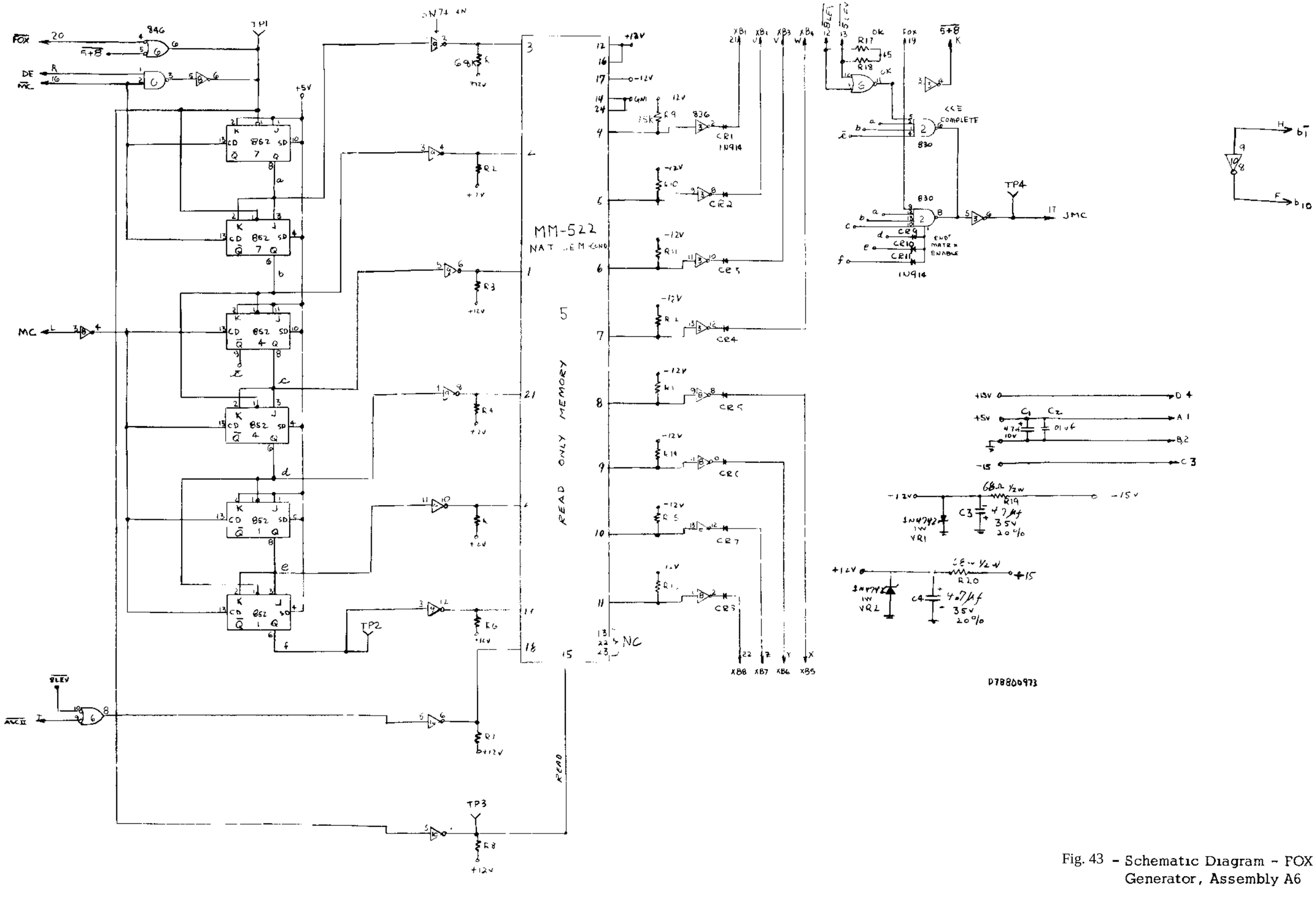


Fig. 42 - Component Locations - FOX Message Generator, Assembly A5



D78800973

Fig. 43 - Schematic Diagram - FOX Message Generator, Assembly A6

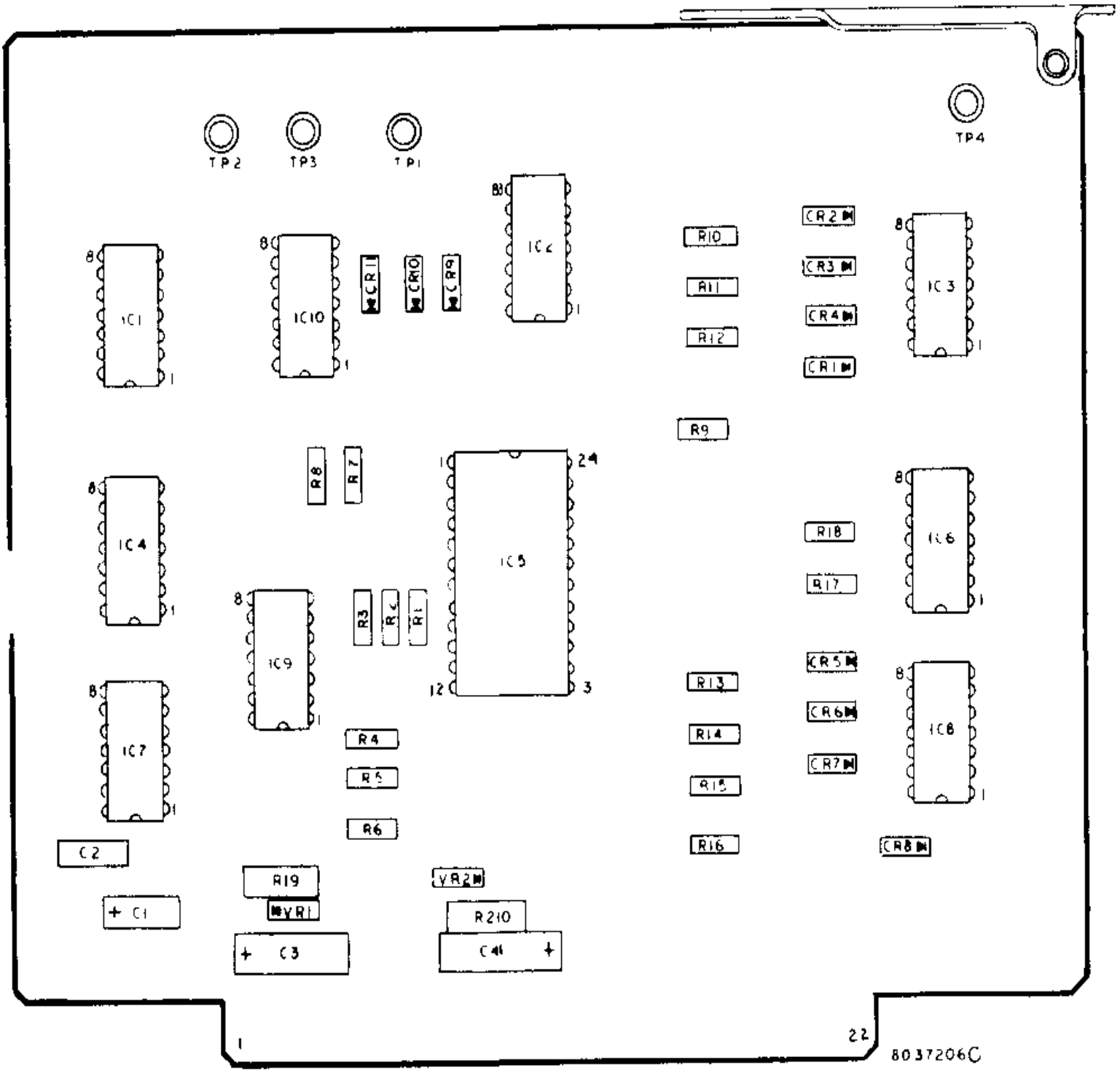
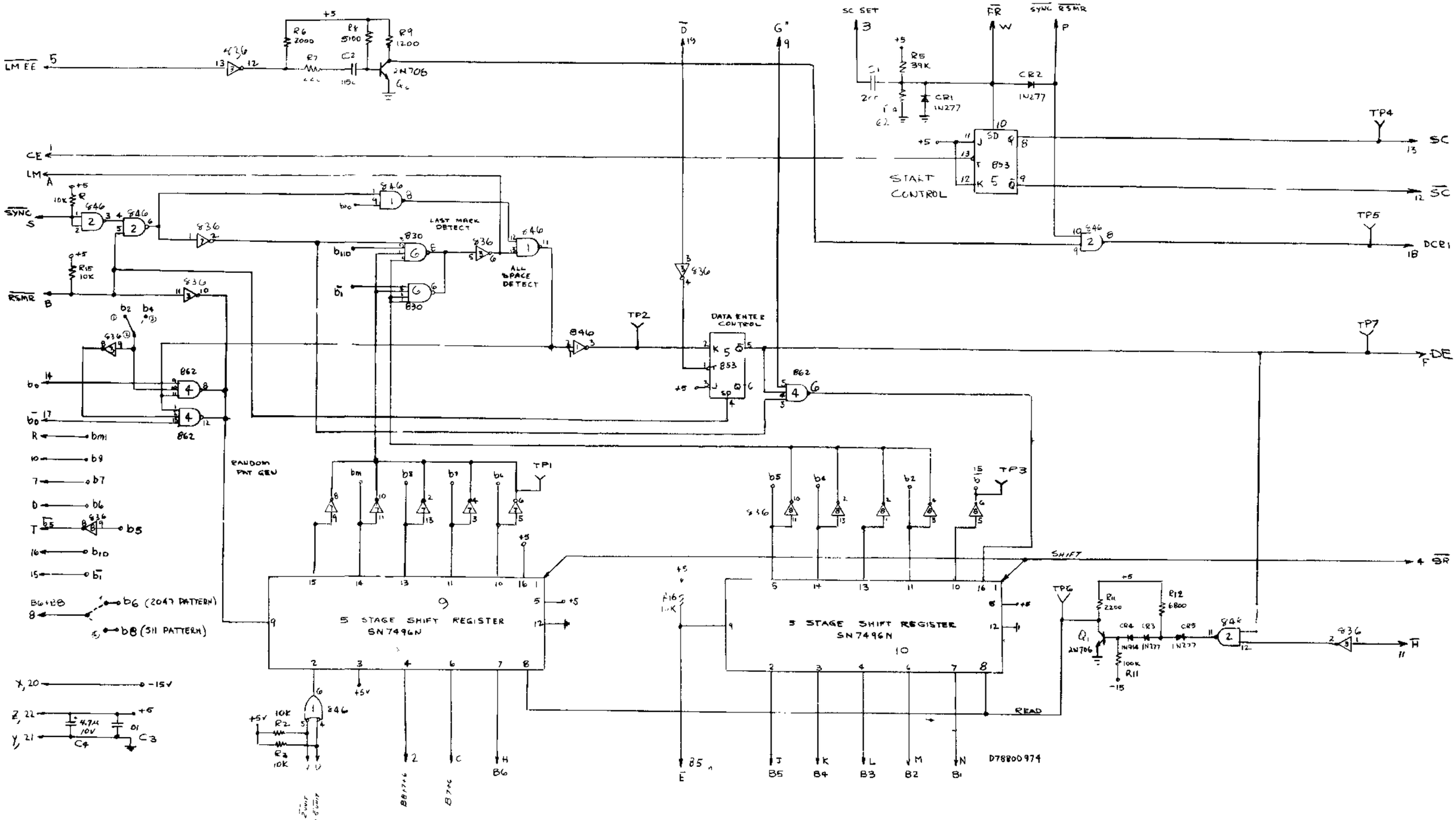


Fig. 44 - Component Locations, FOX Message Generator, Assembly A6



NOTE
511 BIT COMMON PATTERN STRAP 1-2 AND 5-6
511 BIT CCITT PATTERN, STRAP 2-3 AND 5-6
2047 BIT PATTERN STRAP 1-2 AND 4-5.

Fig. 45 - Schematic Diagram - Character Distributor (Data Register) and Timing Control, Assembly A7

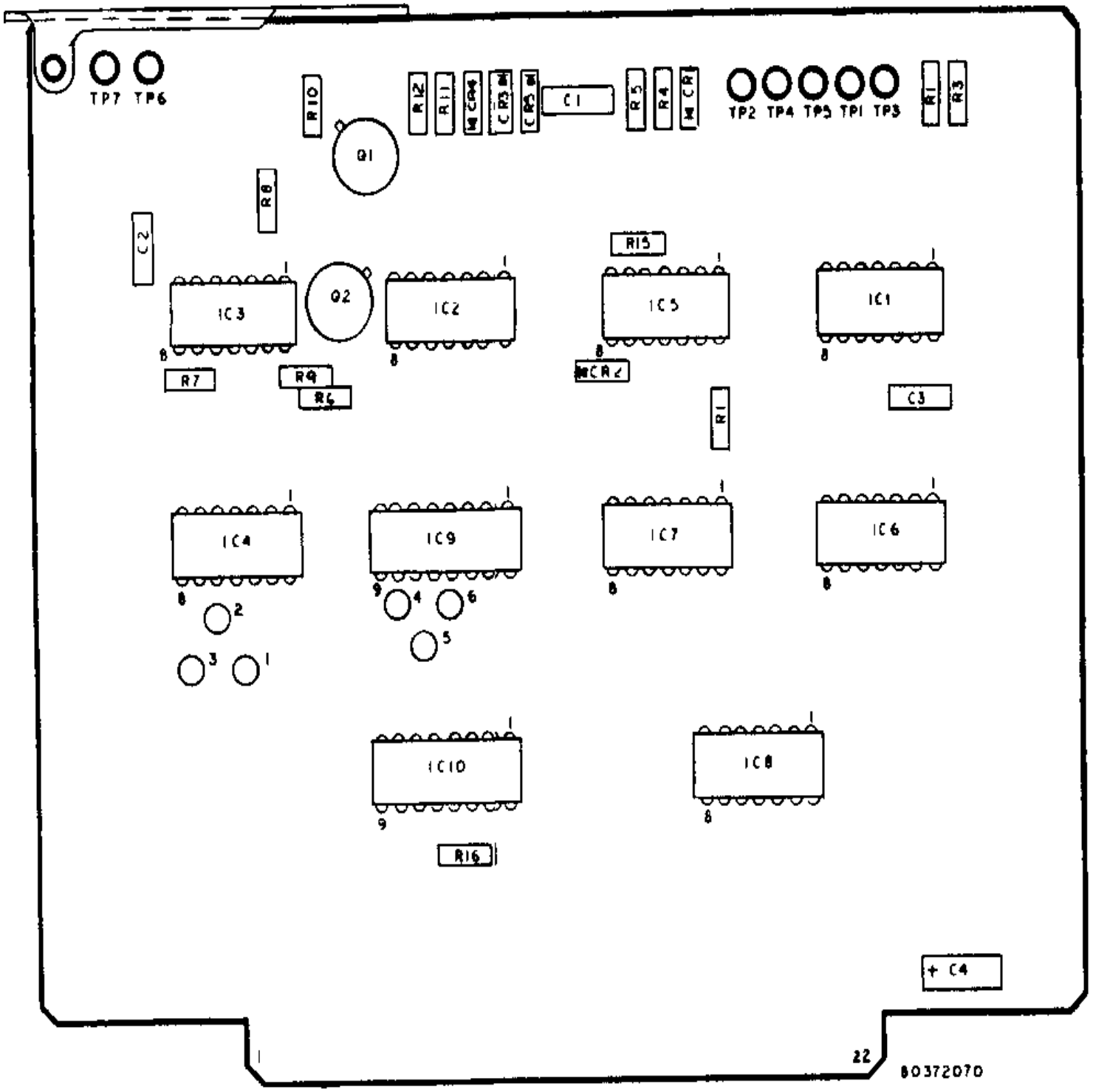


Fig. 46 - Component Locations - Character Distributor (Data Register) and Timing Control, Assembly A7

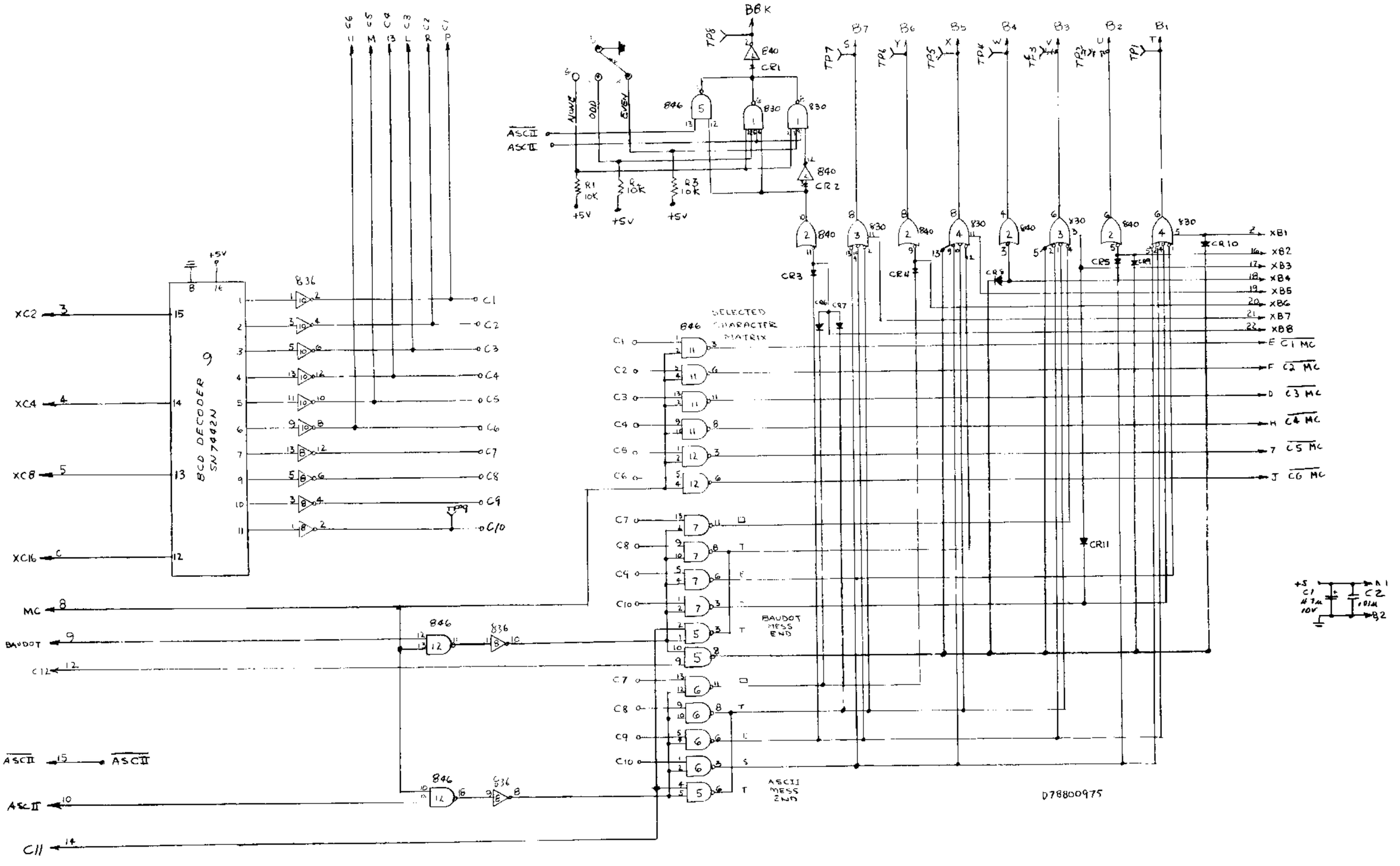


Fig. 47 - Schematic Diagram - Signal Pattern Matrix, Assembly A8

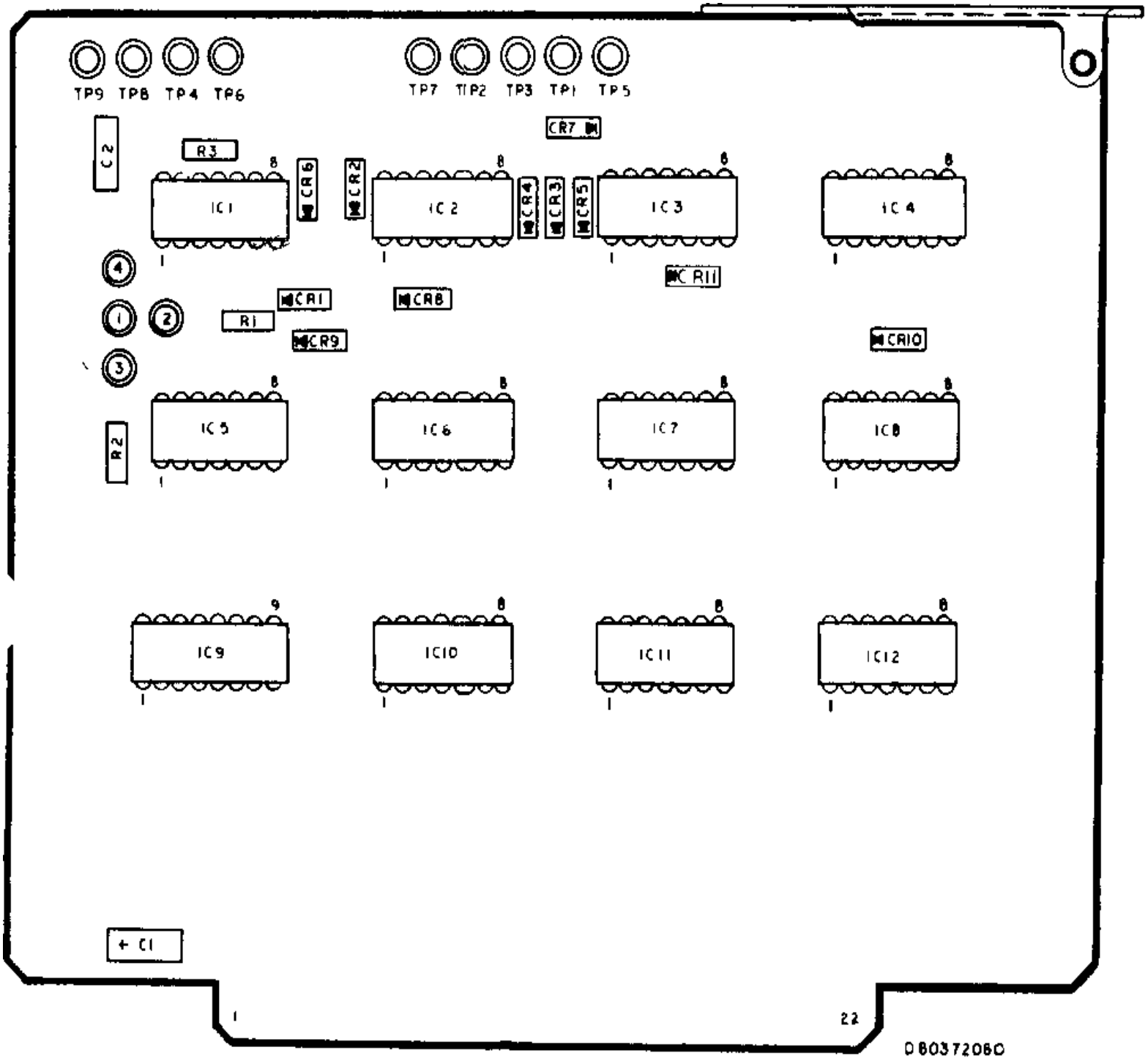


Fig. 48 - Component Locations - Signal Pattern Matrix, Assembly A8

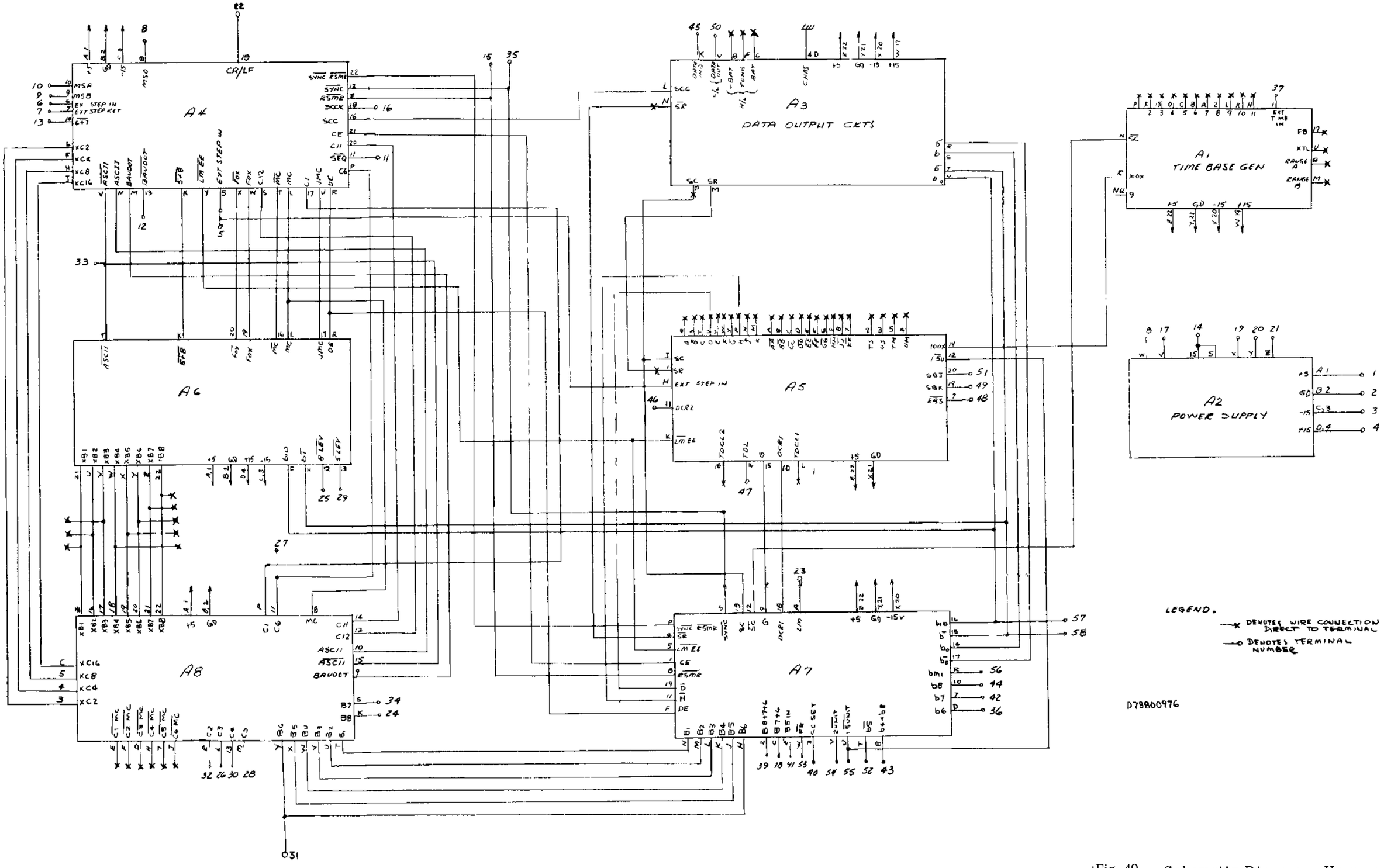


Fig. 49 - Schematic Diagram - Harness Board, Assembly A10

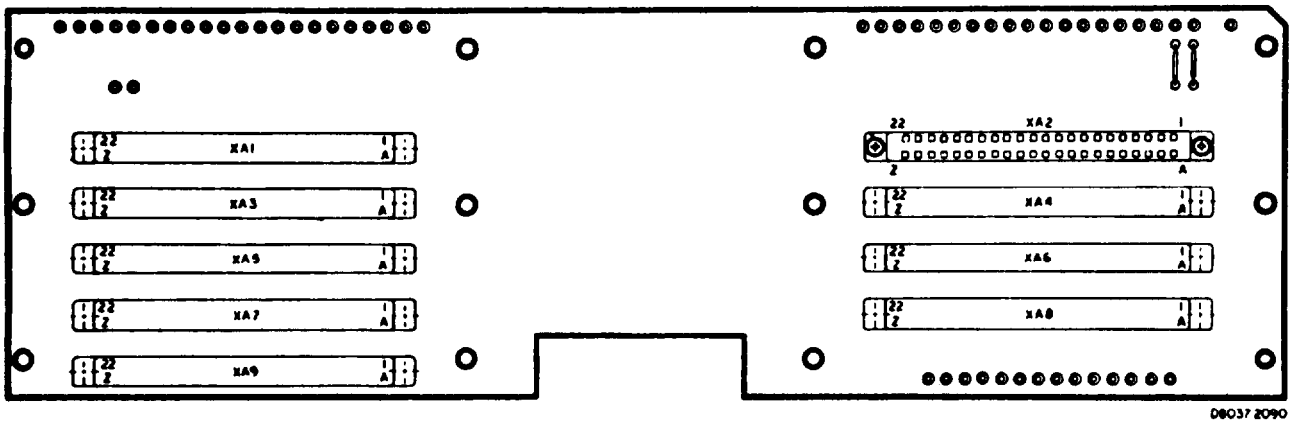


Fig. 50 - Component Locations - Harness Board, Assembly A10

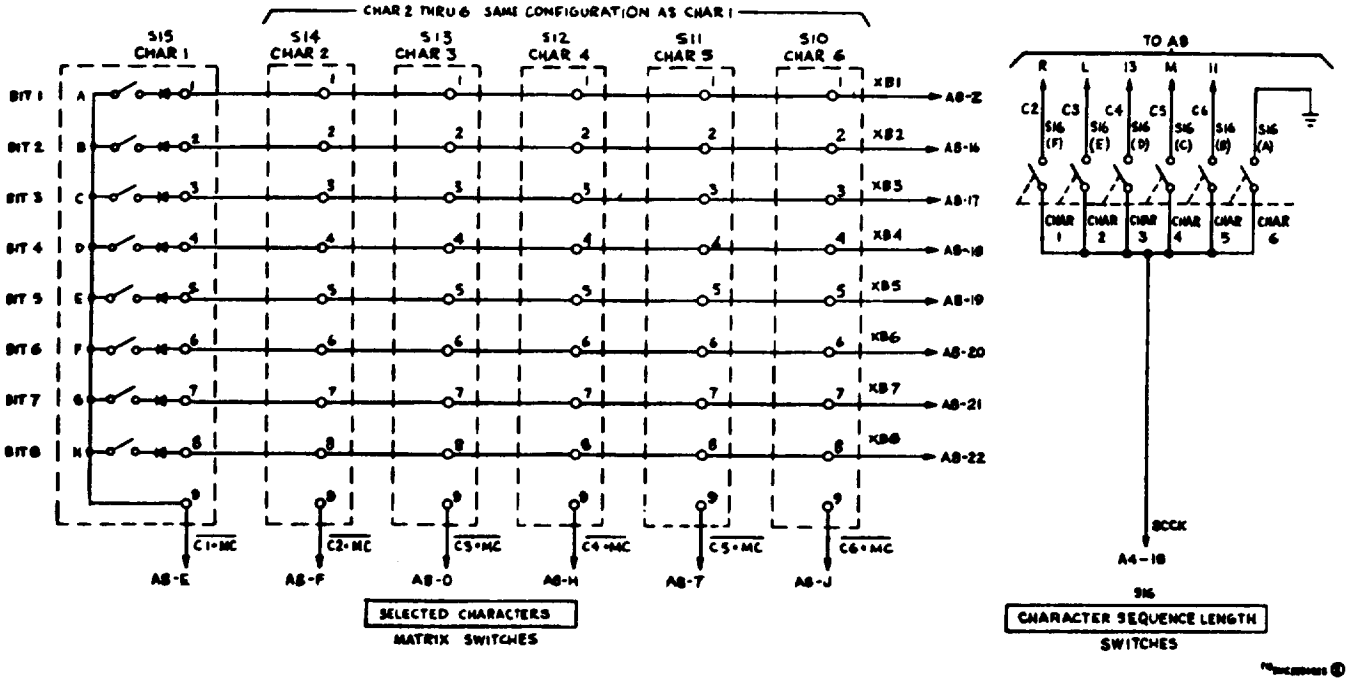


Fig. 51 - Schematic/Wiring Diagram - Selected Character Switches

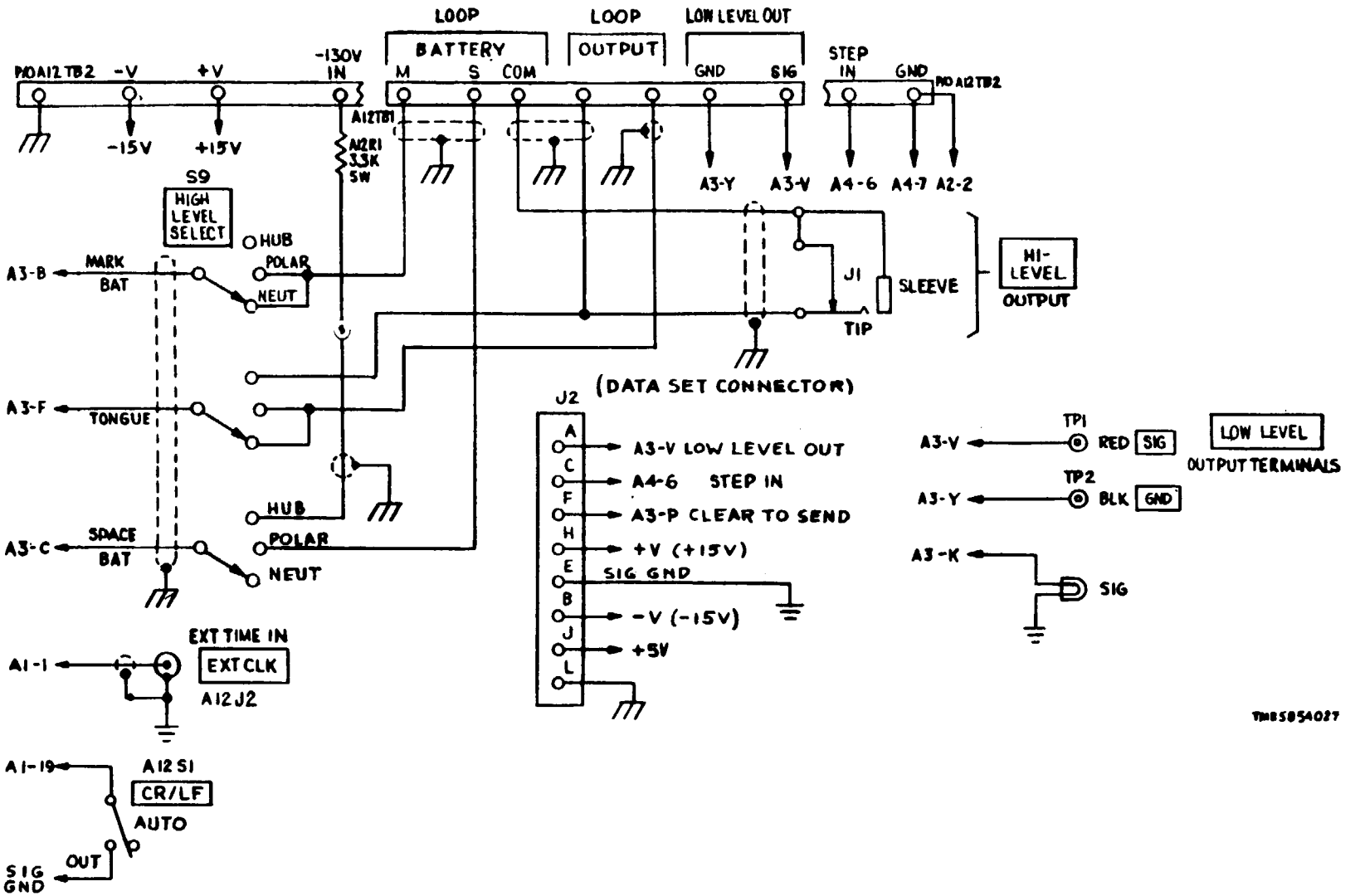
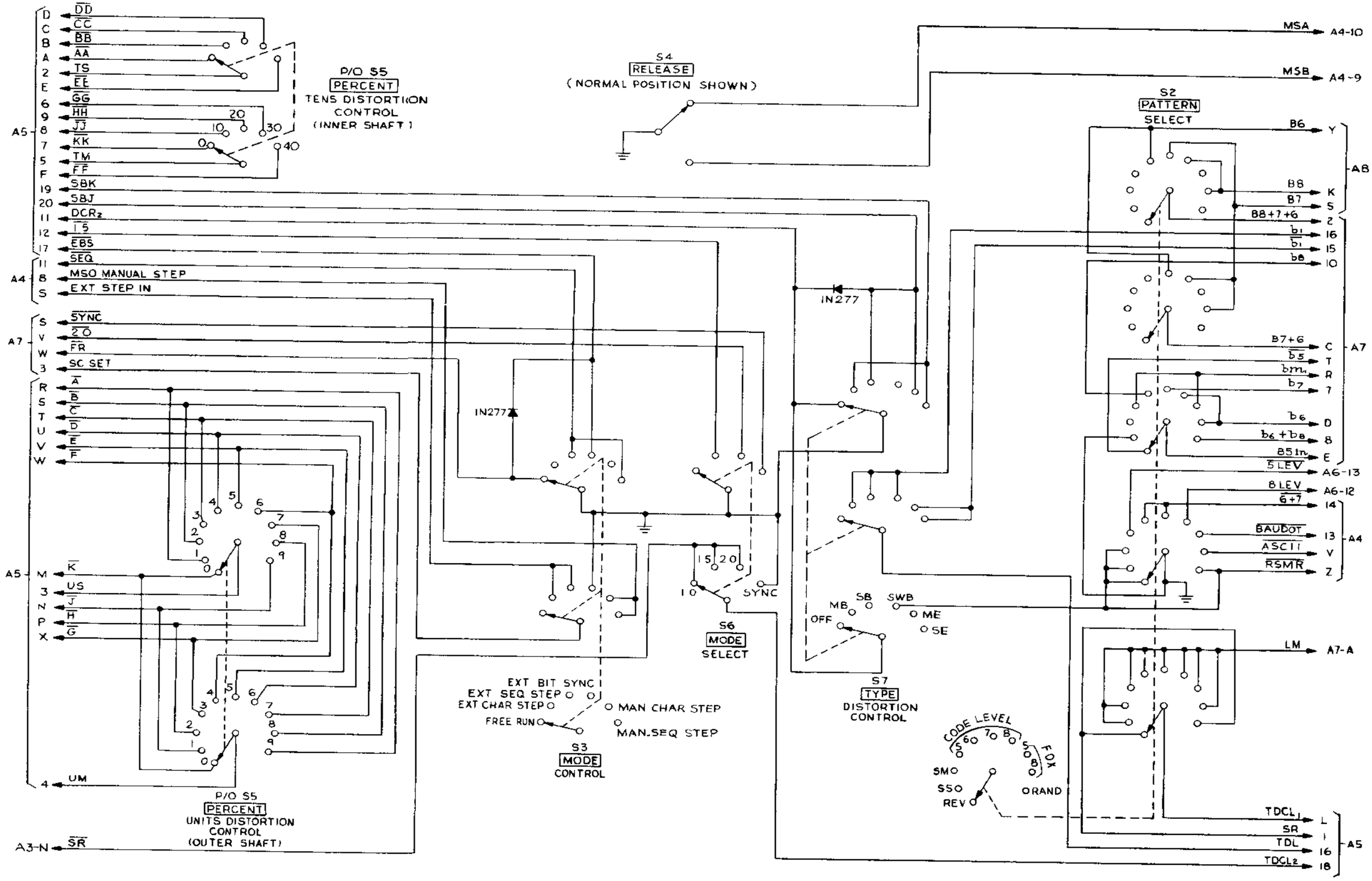


Fig. 52 - Schematic Diagram - Connector and Output Circuitry, Front and Rear Panel



TME5854041

Fig. 53 – Wiring Diagram – Front- Panel Switches

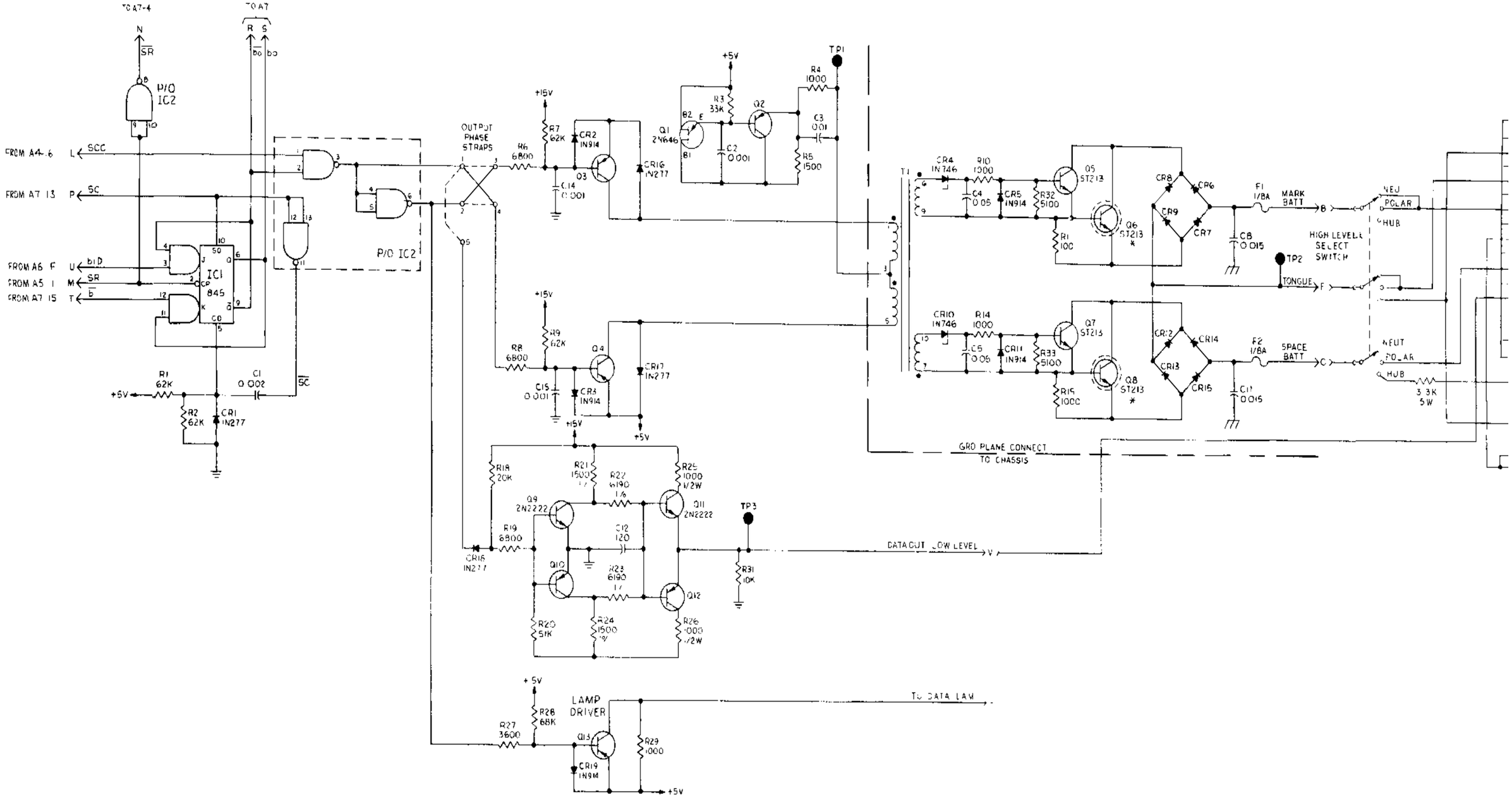
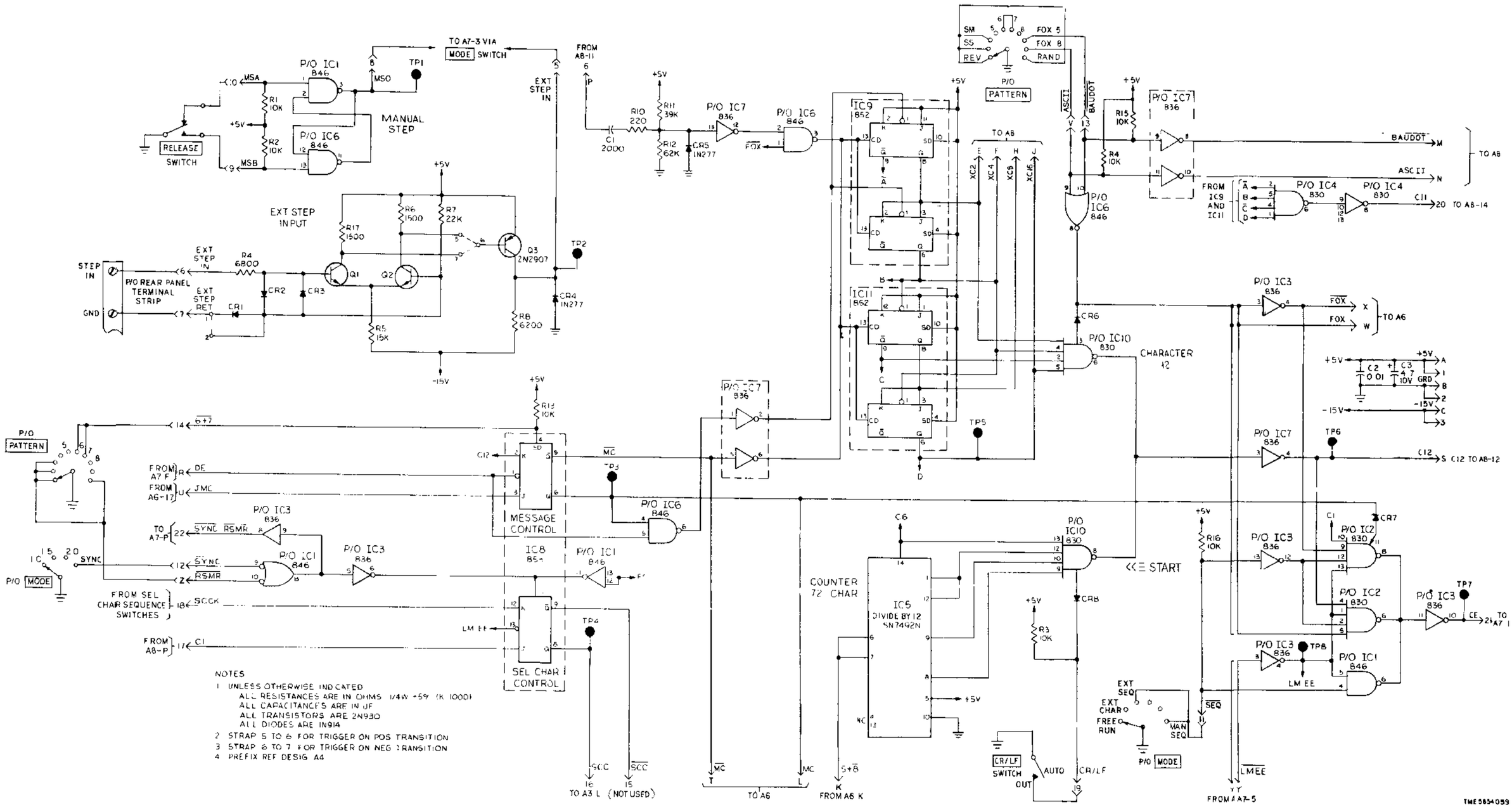


Fig. 54 - Qutput Circ



NOTES

1. UNLESS OTHERWISE INDICATED
   ALL RESISTANCES ARE IN OHMS 1/4W ±5% (K 1000)
   ALL CAPACITANCES ARE IN UF
   ALL TRANSISTORS ARE 2N930
   ALL DIODES ARE IN914
2. STRAP 5 TO 6 FOR TRIGGER ON POS TRANSITION
3. STRAP 6 TO 7 FOR TRIGGER ON NEG TRANSITION
4. PREFIX REF DESIG A4

Fig. 55 - Front- and Rear-Panel Switches/ Assembly A4 Interconnections

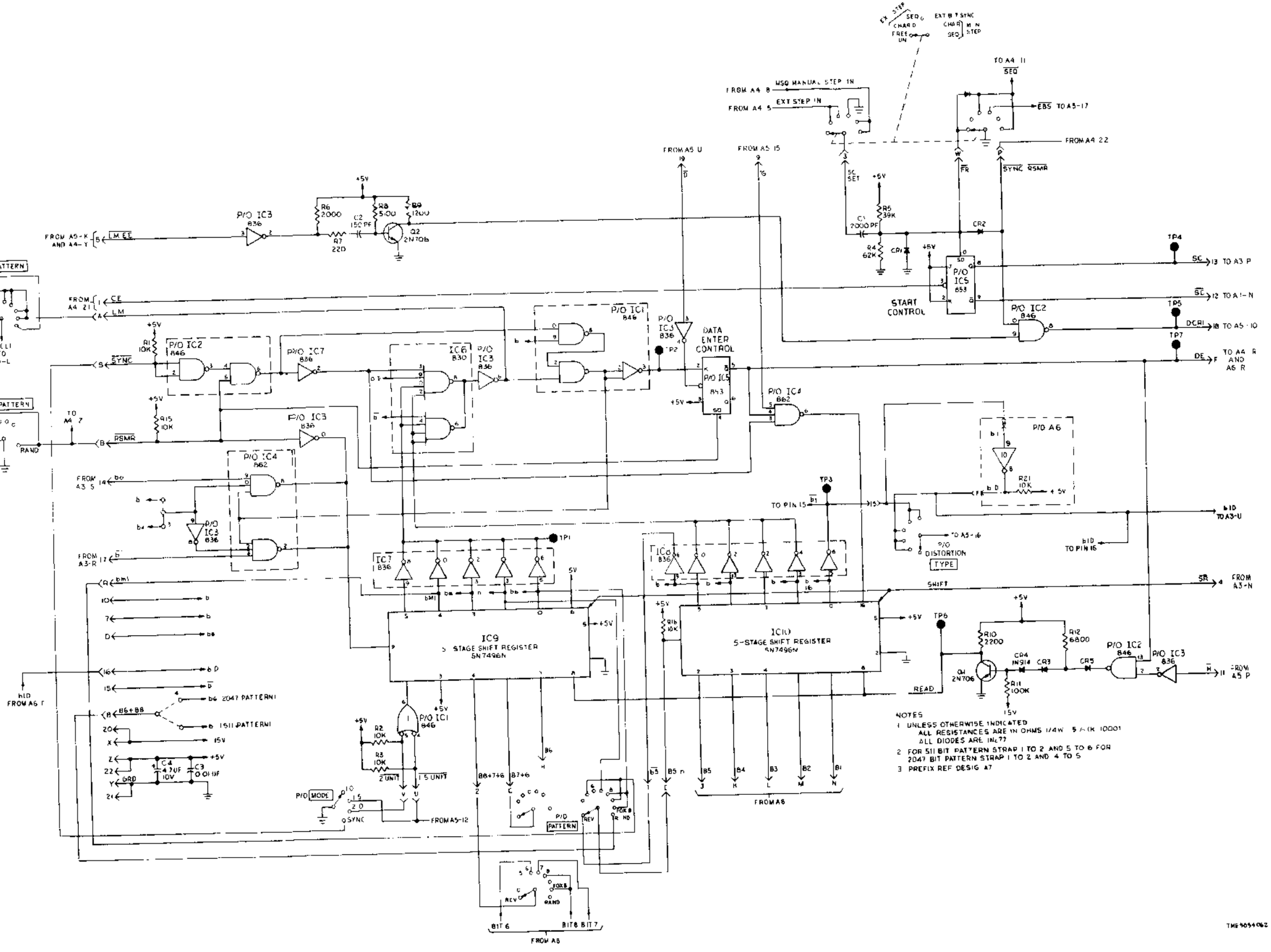


Fig. 56 - Front-Panel Switches/ Assembly A7 Interconnections

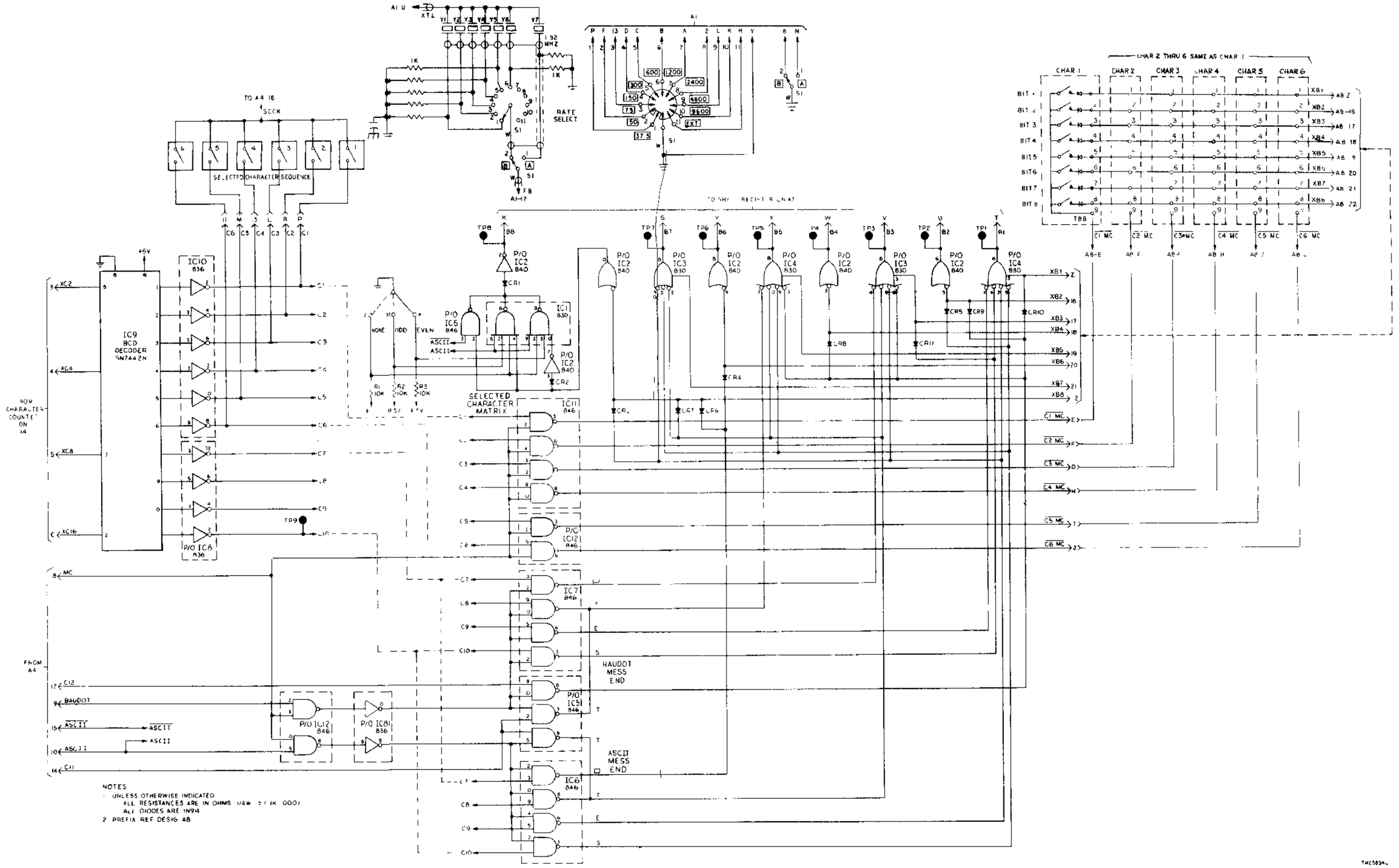


Fig. 57 - Front-Panel Switches/Assembly A1 and A8 Interconnections

5. PARTS LIST

(A) Introduction

5.01 A complete list of replaceable electronic parts for the PG-303A Pattern Generator is presented in (B) below. Table VI consists of an equipment breakdown into assemblies, subassemblies, and detailed parts; Table VII consists of an optional accessories breakdown; and Tables VIII through XXI consist of breakdowns of PC-cards and assemblies into detailed parts. Table XXII cross references commercial part numbers to National Stock Numbers.

(a) Within each table, parts are listed in alphanumeric order, by reference-designation symbol; for each entry, a brief description and the manufacturer part and code number are provided. Manufacturer codes are identified in Table V.

(b) To order a part, note the part number and then cross reference that part number to the National Stock Number in Table XXII; then order through normal ordering channels. If the part number does not have a National Stock Number, then order the part through normal ordering channels using the commercial part number.

TABLE V MANUFACTURER CODES

CODE NO.	MANUFACTURER	
01295	Texas Instruments, Semiconductor Div.	Dallas, Texas
02660	Amphenol Corp.	Broadview, Illinois
03508	General Elec. Co.	Syraçuse, New York
04713	Motorola Semiconductor Products, Inc.	Pheonix, Arizona
12040	Nathonal Semiconductor Corp.	Danbury, Connecticut
21604	Buckeye Stamping Co.	Columbus, Ohio
22753	UID Electronics Corp.	Hollywood, Florida
24446	General Electric Co.	Schenectady, New York
56289	Sprague Electric Co.	North Adams, Massachusetts
71279	Cambridge Thermionic Corp.	Cambridge, Massachusetts
71400	Bussmann Mfg. Co.	St. Louis, Missouri
71450	CTS Corp.	Elkhart, Indiana
71785	Cinch Mfg. Co.	Chicago, Illinois

TABLE V (Cont'd)

CODE NO.	MANUFACTURER	
72136	Electro Motive Mfg. Co.	Williamantic, Connecticut
72619	Dialight Corp.	Brooklyn, New York
74545	Harvey Hubbell, Inc.	Bridgeport, Connecticut
74970	E. F. Johnson Co.	Waseca, Minnesota
75382	Kulica Electric Co.	Mount Vernon, New York
75915	Littelfuse, Inc.	Des Plaines, Illinois
81349	Military Specifications	
82104	Standard Grigsby Co.	Aurora, Illinois
82389	Switchcraft, Inc.	Chicago, Illinois
91418	Radio Materials Co.	Chicago, Illinois
95146	ALCO Electric	Lawrence, Massachusetts
96228	STELMA, Inc.	Stamford, Connecticut

(B) Parts List, Tabular Listing

5.02 Refer to Tables VIII through XXI for parts lists of Pattern Generator components listed in Table VI and of accessory items listed in Table VII.

TABLE VI

PATTERN GENERATOR, PG-303A: 90372003-000

REF DESIG	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
A1	CKT CARD ASSY,TIME BASE LOGIC:	80372010-000	96238
A2	CKT CARD ASSY,POWER SUPPLY:	80372020-000	96238
A3	CKT CARD ASSY,DATA OUTPUT CKT, Hi, Lo:	80372030-000	96238
A4	CKT CARD ASSY,MESSAGE CONT CKT:	80372040-000	96238
A5	CKT CARD ASSY, DISTORTION GENERATOR:	80372050-000	96238
A6	CKT CARD ASSY,MESSAGE GENERATOR:	80372060-000	96238
A7	CKT CARD ASSY,DISTR & TIMING CONTROL	80372070-000	96238

TABLE VI (CONT'D)

REF DESIG	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
A8	CKT CARD ASSY,SIGNAL PATTERN MATRIX	80372080-000	96238
A9	CKT CARD ASSY,EXTENDER CARD:	80372180-000	96238
A10	CKT CARD ASSY,PATTERN GEN HARNESS CARD:	80372090-000	96238
A11	CRYSTAL BRACKET ASSY:	90372006-000	96238
A12	POWER SUPPLY,PATTERN GEN:	90372004-000	96238
A13	LINE CORD ASSY:	74000054-000	96238
A13P1	CONN,PLUG,ELEC:	7571	74545
A13W1	CABLE ASSY,PWR:	74000000-002	96238
A14	CKT CARD ASSY: SEL SWITCH	80372200-000	96238
DS1	LIGHT,INDICATOR: COLORLESS LENS	507-3905-1437-500	72619
J1	JACK,TELEPHONE:	N112A	82389
J2	CONN,RCPT. ELEC: 12 PIN	90372005-000	96238
MP1	KNOB FOR S1	PS70D95C1BLK	21604 2BLK
MP2,3,6 7,9	KNOB FOR S2,S3,S7, AND S9	PS70BLS2BLK	21604
MP5	KNOB FOR S5, MODIFIED	57025147-000	96238
MP10-MP15	PUSHBOTTON FOR S10 THROUGH S15	400/3	82104
MP16,17	HANDLE	56025087-000	96238
S1	(P/O A11 ASSY 90372006-000)		
S2	SWITCH,ROTARY: 4 POLE, 10 POS	46020389-000	96238
S3	SWITCH,ROTARY: 3 POLE, 6 POS	46020386-000	96238
S4	SWITCH,PB: SPDT, 115 VAC MOM.	MSP105F	95146
S5	SWITCH,ROTARY: 2 POLE, 5-10 POS	46020391-000	96238
S6	SWITCH,ROTARY: 2 POLE, 4 POS	46020397-000	96238
S7	SWITCH,ROTARY: 2 POLE, 6 POS	46020383-000	96238
S8	SWITCH,ROCKER:	LRSW322N30KCR	22753
S9	SWITCH,ROTARY: 3 POLE, 3 POS	46020388-000	96238
S10-S15	(USED ON A14 80372200-000)		
S16	SWITCH,PB:	46027640-000	96238
TP1	POST,BINDING: RED	111-102	74970
TP2	POST,BINDING: BLACK	111-103	74970
XDS1	SOCKET,IND LIGHT:	515-0012	72619
Y1-Y6	FREQUENCY VALUES OF CRYSTALS IS DETERMINED BY THE RATE SPECIFIED BY THE CUSTOMER		
Y7	XTAL UNIT, QTZ: 1.920MHZ	40040081-000	96238

TABLE VII

ACCESSORY ITEMS: (OPTIONAL)

REF DESIG	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
	CASE AND COVER ASSEMBLY	64030083-000	96238
	DIAL ASSEMBLY:	57025141-000	96238
Y1	XTAL UNIT,QTZ: 291.200KHZ	40040082-001	96238
Y2	XTAL UNIT,QTZ: 363.712KHZ	40040082-002	96238
Y3	XTAL UNIT,QTZ: 391.296KHZ	40040082-004	96238
Y4	XTAL UNIT,QTZ:474.880KHZ	40040082-006	96238
Y5	XTAL UNIT,QTZ: 352.000KHZ	40040082-003	96238
Y6	XTAL UNIT,QTZ: 430.400KHZ	40040082-005	96238
	(DIAL ASSY 57025141-000 AND CRYSTALS Y1-Y6 ARE USED SIMULTANEOUSLY)		
	DIAL ASSEMBLY:	57000021-000	96238
Y1-Y6	(CRYSTALS SPECIFIED BY CUSTOMER)		

TABLE VIII
CIRCUIT CARD ASSEMBLY, TIME-BASE LOGIC: A1, 80372010-00

REF DESIG	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
A1	CKT CARD ASSY,OSCILLATOR:	80372190-000	96238
C1,C2	CAP,FXD,CERAMIC: 0.0LUF, ±35%, 100V	TA01UF	91418
C3	CAP,FXD,ELCTLT: 4.7UF, ±20% 10V	CS13BC475M	81349
CR1,CR2	SEMICOND,DIODE: SILICON	1N914	81349
CR3-CR5	SIMICOND,DIODE: GERMANIUM	1N277	81349
CR6	SAME AS CR1		
IC1,IC2	INTEGRATED CKT: NAND/NOR GATE	SN15849N	01295
IC3,IC4	INTEGRATED CKT: NAND/NOR GATE	MC858P	04713
IC5,IC6	INTEGRATED CKT: QUAD 2-INPUT NAND/ NOR GATE	SN15846N	01295
IC7	INTEGRATED CKT: DUAL J-K CLOCKED FLIP-FLOP	SN158097N	01295
IC8	INTEGRATED CKT: DUAL J-K CLOCKED FLIP-FLOP	SN158099N	01295

TABLE VIII (CONT'D)

REF DESIG	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
IC9	INTEGRATED CKT: DUAL J-K CLOCKED FLOP-FLOP	SN158094N	01295
IC10	INTEGRATED CKT: 4 BIT BINARY COUNTER	SN7493N	01295
Q1	TRANSISTOR: NPN	2N2222	81349
Q2	TRANSISTOR: NPN	2N706	81349
Q3	SAME AS Q1		
R1	RES,FXD,COMP: 6.8 OHMS, ±5%, 1/4W	RC07GF682J	81349
R2	RES,FXD,COMP: 2.2K OHMS, ±5%, 1/4W	RC07GF222J	81349
R3	RES,FXD,COMP: 1K OHMS, ±5%, 1/4W	RC07GF102J	81349
R4-R16	RES,FXD,COMP: 10K OHMS, ±5%, 1/4W	RC07GF103J	81349
R17	SAME AS R3		
R18	RES,FXD,COMP: 3K OHMS, ±5%, 1/4W	RC07GF302J	81349
R19	RES,FXD,COMP: 47K OHMS, ±5%, 1/4W	RC07GF473J	81349
R20	SAME AS R18		

TABLE IX
CIRCUIT CARD ASSEMBLY, OSCILLATOR: A1A1, 80372190-000

REF DESIG	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
C1	CAP,FXD,CERAMIC: 0.0LUF, ±35% 100V	TA01UF	91418
C2	CAP,FXD,CERAMIC: 0.1UF, ±20% 25V	5C023104X0250B3	56289
C3-C8	NOT USED		
C9,C10	SAME AS C1		
CR1	SEMICOND,DIODE: SILICON	1N914	81349
CR2-CR5	SEMICOND,DIODE: GERMANIUM	1N277	81349
Q1	TRANSISTOR: PNP	2N2907	81349
Q2,Q3	TRANSISTOR:	2N5222	04713
Q4	TRANSISTOR: NPN	2N706	81349
Q5	TRANSISTOR: NPN	2N2222	81349
Q6	SAME AS Q4		
R1	RES,FXD,COMP: 8.2K OHMS, ±5%, 1/4W	RC07GF822J	81349
R2	RES,FXD,COMP: 3K OHMS, ±5%, 1/4W	RC07GF302J	81349
R3	RES,FXD,COMP: 3.1K OHMS, ±5%, 1/4W	RC07GF512J	81349
R4	RES,FXD,COMP: 3.3K OHMS, ±5%, 1/4W	RC07GF332J	81349
R5	RES,FXD,COMP: 39K OHMS, ±5%, 1/4W	RC07GF393J	81349
R6	RES,FXD,COMP: 18K OHM, ±5%, 1/4W	RC07GF183J	81349
R7-R11	NOT USED		

TABLE IX (CONT'D)

REF DESIG	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
R12	RES,FXD,COMP: 15K OHMS, ±5%, 1/4W	RC07GF153J	81349
R13	RES,FXD,COMP: 2.4K OHMS, ±5%, 1/4W	RC07GF242J	81349
R14	RES,FXD,COMP: 100 OHMS, ±5%, 1/4W	RC07GF101J	81349
R15	RES,FXD,COMP: 10K OHMS, ±5%, 1/4W	RC07GF103J	81349
R16	RES,FXD,COMP: 2K OHMS, ±5%, 1/4W	RC07GF202J	81349

TABLE X
CIRCUIT CARD ASSEMBLY,POWER SUPPLY: A2 80372020-000

REF DESIG	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
C1,C2	CAP,FXD,ELCTLT: 260UF, 30V	39D257G030EL4	56289
C3	CAP,FXD,ELCTLT: 15UF, ±10%, 35V	CS13BF156K	81349
C4	CAP,FXD,ELCTLT: 1UF, ±10%, 35V	CS13BF105K	81349
C5	SAME AS C3		
C6	CAP,FXD,MICA: 4700PF, ±5%, 500V	DM19E472J0500 WV4CR	72136
C7	CAP,FXD,MICA: 560PF, ±10%, 500V	DM15F561K0500 WV4CR	72136
C8	CAP,FXD,ELCTLT: 22UF, ±10%, 35V	CS13BF226K	81349
C9,C10	SAME AS C3		
CR1-CR4	SEMICOND,DIODE: SILICON	1N645	81349
CR5,CR6	SEMICOND,DIODE: SILICON	1N1614	81349
CR7	RECTIFIER,SILICON:	C106Q21	03508
F1,F2	FUSE,CARTRIDGE: 1/8 AMP	312-125	75915
F3	FUSE,CARTRIDGE: 3/4 AMP	312-750	75915
Q1	TRANSISTOR: NPN	2N1613	81349
Q2	TRANSISTOR: NPN	2N930	81349
Q3,Q4	TRANSISTOR: PNP	2N2905	81349
Q5	TRANSISTOR: PNP	2N297	81349
Q6	SAME AS Q1		
Q7,Q8	SAME AS Q2		
Q9	SAME AS Q3		
R1	RES,FXD,COMP: 39 OHMS, ±5%, 2W	RC42GF390J	81349
R2-R4	RES,FXD,COMP: 1K OHMS, ±5%, 1/4W	RC07GF102J	81349
R5	RES,FXD,COMP: 1.5K OHMS, ±5%, 1/4W	RC07GF152J	81349
R6	RESISTOR,VAR:500 OHMS, 1/4W	200P1-501	80294

TABLE X (CONT'D)

REF DESIG	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
R7	SAME AS R2		
R8	RES,FXD,COMP: 6.8K OHMS, ±5%, 1/4W	RC07GF682J	81349
R9	RES,FXD,COMP: 680 OHMS, ±5%, 1/2W	RC20GF681J	81349
R10	SAME AS R1		
R11-R13	SAME AS R2		
R14	SAME AS R8		
R15	RES,FXD,COMP: (FACTORY SELECT)		
R16	RES,FXD,WW: 1 OHMS, ±5%, 5W	RW67V1R0	81349
R17	RES,FXD,COMP: 180 OHMS, ±5%, 1/4W	RC07GF181J	81349
R18	RES,FXD,COMP: 560 OHMS, ±5%, 1/4W	RC07GF561J	81349
R19	RES,FXD,COMP: 22 OHMS, ±5%, 1/2W	RC20GF220J	81349
R20	RES,FXD,FILM: 453 OHMS, ±10%, 1/8W	RN55D4530F	81349
R21	RESISTOR,VAR: 200 OHMS, 1/4W	200P1-201	80294
R22	RES,FXD,FILM: 732 OHMS, ±1%, 1/8W	RN55D7320F	81349
R23	RES,FXD,COMP: 2.2K OHMS, ±5%, 1/4W	RC07GF222J	81349
R24	RES,FXD,COMP: 4700 OHMS, ±5%, 1/4W	RC07GF471J	81349
R25	SAME AS R18		
R26	RES,FXD,COMP: 620 OHMS, ±5%, 1/4W	RC07GF621J	81349
R27,R28	SAME AS R2		
R29	RES,FXD,COMP: 680 OHMS, ±5%, 1/4W	RC07GF681J	81349
VR1	SEMICOND,DIODE: ZENER	1N752	81349
VR2	SEMICOND,DIODE: ZENER	1N748	81349
VR3	SAME AS VR1		

TABLE XI
CIRCUIT CARD ASSEMBLY, DATA OUTPUT CIRCUITS HI-LO LEVEL: A3, 8037203-0-000

REF DESIG	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
C1	CAP,FXD,CERAMIC: 2000PF, 1000V	DD202	71590
C2	CAP,FXD,CERAMIC: 0.00LUF, ±20%, 1000V	5GAD10	56289
C3	CAP,FXD,CERAMIC: 0.0LUF, ±35%, 100V	TA01UF	91418
C4,C5	CAP,FXD,CERAMIC: 0.05UF, ±20%, 100V	TGS50	56289
C6,C7	NOT USED		
C8	CAP,FXD,CERAMIC: 0.015UF, ±20%, 1000V	CCD153	72136
C9,C10	NOT USED		
C11	SAME AS C8		
C12	CAP,FXD,MICA: 120PF, ±10% 500V	DM15E121K0500 WV4CR	72136

TABLE XI (CONT'D)

REF DESIG	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
C13	CAP,FXD,ELCTLT: 4.7UF, ±20% 10V	CS13BC475M	81349
C14,C15	SAME AS C2		
C16	SAME AS C3		
C17	CAP,FXD,ELCTLT: 4.7UF, ±20%, 35V	CS13BF475M	81349
CR1	SEMICOND,DIODE: GERMANIUM	1N277	81349
CR2,CR3	SEMICOND,DIODE: SILICON	1N914	81349
CR4	SEMICOND,DIODE: ZENER	1N746	81349
CR5	SAME AS CR2		
CR6-CR9	SEMICOND,DIODE: SILICON	1N647	81349
CR10	SAME AS CR4		
CR11	SAME AS CR2		
CR12-CR15	SAME AS CR6		
CR16-CR18	SAME AS CR1		
CR19	SAME AS CR2		
F1,F2	FUSE,CARTRIDGE: 1/8 AMP	312-125	75915
IC1	INTEGRATED CKT: FLIP-FLOP	SN15845N	01295
IC2	INTEGRATED CKT: QUAD 2-INPUT NAND GATE	SN15846N	01295
Q1	TRANSISTOR: UNIJUNCTION	2N2646	04713
Q2-Q4	TRANSISTOR: PNP	2N2905	81349
Q5-Q8	TRANSISTOR: NPN	40001213-000	96238
Q9	TRANSISTOR:	2N2222	81349
Q10	SAME AS Q2		
Q11	SAME AS Q9		
Q12,Q13	SAME AS Q2		
R1,R2	RES,FXD,COMP: 62K OHMS, ±5%, 1/4W	RC07GF623J	81349
R3	RES,FXD,COMP: 33K OHMS, ±5%, 1/4W	RC07GF333J	81349
R4	RES,FXD,COMP: 1K OHMS, ±5%, 1/4W	RC07GF102J	81349
R5	RES,FXD,FILM: 1.5K OHMS, ±1% 1/8W	RN55D1501F	81349
R6	RES,FXD,COMP: 6.8K OHMS, ±5%, 1/4W	RC07GF682J	81349
R7	SAME AS R1		
R8	SAME AS R6		
R9	SAME AS R1		
R10	RES,FXD,COMP: 1K OHMS, ±5%, 1/2W	RC20GF102J	81349
R11	RES,FXD,COMP: 100 OHMS, ±5%, 1/4W	RC07GF101J	81349
R12,R13	NOT USED		
R14	SAME AS R10		
R15	SAME AS R11		

TABLE XI (CONT'D)

REF DESIG	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
R16,R17	NOT USED		
R18	RES,FXD,COMP: 20K OHMS, ±5%, 1/4W	RC07GF203J	81349
19	SAME AS R6		
20	RES,FXD,COMP: 51K OHMS, ±5%, 1/4W	RC07GF513J	81349
R21	SAME AS R5		
R22,R23	RES,FXD,FILM: 6190 OHMS, ±1%, 1/8W	RN55D6191F	81349
R24	SAME AS R5		
R25,R26	SAME AS R10		
R27	RES,FXD,COMP: 3.6K OHMS, ±5%, 1/4W	RC07GF362J	81349
R28	RES,FXD,COMP: 68K OHMS, ±5%, 1/4W	RC07GF683J	81349
R29	SAME AS R4		
R30	NOT USED		
R31	RES,FXD,COMP: 10K OHMS, ±5%, 1/4W	RC07GF103J	81349
R32,R33	RES,FXD,COMP: 5.1K OHMS, ±5%, 1/4W	RC07GF512J	81349
R34,R35	RES,FXD,COMP: 3K OHMS, ±5%, 1/4W	RC07GF302J	81349
T1	TRANSFORMER, PULSE: 500V, 60HZ	43003041-000	96238

TABLE XII

CIRCUIT CARD ASSEMBLY, MESSAGE CONTROL CIRCUITS: A4, 80372040-000

REF DESIG	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
C1	CAP,FXD,CERAMIC: 2000PF, 1000V	DD202	71590
C2	CAP,FXD,CERAMIC: 0.01UF, ±35%, 100V	TA01UF	91418
C3	CAP,FXD,ELCTLT: 4.7UF, ±20%, 10V	CS13BC475M	81349
CR1-CR3	SEMICOND,DIODE: SILICON	1N914	81349
CR4,CR5	SEMICOND,DIODE: GERMANIUM	1N277	81349
CR6,CR7	SAME AS CR1		
IC1	INTEGRATED CKT: QUAD 2-INPUT NAND GATE	SN15846N	01295
IC2	INTEGRATED CKT: HEX INVERTER NAND GATE	SN15830N	01295
IC3	INTEGRATED CKT: HEX INVERTER	SN15836N	01295
IC4	SAME AS IC2		
IC5	INTEGRATED CKT: DIVIDE BY 12 COUNTER	SN7492N	01295
IC6	SAME AS IC1		
IC7	SAME AS IC3		
IC8	INTEGRATED CKT: DUAL J-K CLOCKED FLIP-FLOP	SN158093N	01295

TABLE XII (CONT'D)

REF DESIG	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
IC9	INTEGRATED CKT: DUAL J-K CLOCKED FLIP-FLOP	SN158099N	01295
IC10	SAME AS IC2		
IC11	SAME AS IC9		
Q1,Q2	TRANSISTOR: NPN	2N930	81349
Q3	TRANSISTOR: PNP	2N2907	81349
R1,R2	RES,FXD,COMP: 10K OHMS, ±5%, 1/4W	RC07GF103J	81349
R3	NOT USED		
R4	RES,FXD,COMP: 6.8K OHMS, ±5%, 1/4W	RC07GF682J	81349
R5	RES,FXD,COMP: 15K OHMS, ±5%, 1/4W	RC07GF153J	81349
R6	RES,FXD,COMP: 1.5K OHMS, ±5%, 1/4W	RC07GF152J	81349
R7	RES,FXD,COMP: 22K OHMS, ±5%, 1/4W	RC07GF223J	81349
R8	RES,FXD,COMP: 6.2K OHMS, ±5%, 1/4W	RC07GF622J	81349
R9	NOT USED		
R10	RES,FXD,COMP: 220 OHMS, ±5%, 1/4W	RC07GF221J	81349
R11	RES,FXD,COMP: 39K OHMS, ±5%, 1/4W	RC07GF393J	81349
R12	RES,FXD,COMP: 62K OHMS, ±5%, 1/4W	RC07GF623J	81349
R13-R16	SAME AS R1		
R17	SAME AS R6		

TABLE XIII

CIRCUIT CARD ASSEMBLY, DISTORTION GENERATOR: A5, 80372050-000

REF DESIG	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
C1	CAP,FXD,CERAMIC: 0.01UF, ±35%, 100V	TA01UF	91418
C2	CAP,FXD,ELCTLT: 4.7UF, ±20%, 10V	CS13BC475M	81349
C3	CAP,FXD,MICA: 100PF, ±5%, 500V	DM15F101J0500 WV4CR	72136
CR1-CR4	SEMICOND,DIODE: SILICON	1N914	81349
CR5	SEMICOND,DIODE: GERMANIUM	1N277	81349
IC1,IC2	INTEGRATED CKT: HEX INVERTER	SN15836N	01295
IC3	INTEGRATED CKT: DUAL J-K CLOCKED FLIP-FLOP	SN158093N	01295
IC4	INTEGRATED CKT: QUAD 2-INPUT NAND GATE	SN15846N	01295
IC5,IC6	INTEGRATED CKT: DUAL 4-INPUT EXP. NAND GATE	SN15830N	01295
IC7	INTEGRATED CKT: DECADE COUNTER	SN7490N	01295

TABLE XIII (CONT'D)

REF DESIG	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
IC8	SAME AS IC1		
IC9	SAME AS IC7		
IC10	SAME AS IC1		
IC11	INTEGRATED CKT: BCD-TO-DECIMAL 4-10 LINE DECODER	SN7442N	01295
IC12	SAME AS IC4		
IC13	SAME AS IC11		
Q1	TRANSISTOR: SILICON	2N708	81349
R1	RES,FXD,COMP: 2K OHMS, ±5%, 1/4W	RC07GF202J	81349
R2	RES,FXD,COMP: 5.1K OHMS, ±5%, 1/4W	RC07GF512J	81349
R3	RES,FXD,COMP: 220 OHMS, ±5%, 1/4W	RC07GF221J	81349
R4	RES,FXD,COMP: 1.2K OHMS, ±5%, 1/4W	RC07GF122J	81349
R5-R14	RES,FXD,COMP: 10K OHMS, ±5%, 1/4W	RC07GF103J	81349

TABLE XIV

CIRCUIT CARD ASSEMBLY, MESSAGE GENERATOR: A6, 80372060-000

C1	CAP,FXD,ELCTLT: 4.7UF, ±20%, 10V	CS13BC475M	81349
C2	CAP,FXD,CERAMIC: 0.01UF, ±35%, 100V	TA01UF	91418
C3,C4	CAP,FXD,ELCTLT: 4.7UF, ±20%, 35V	CS13AF4R7M	81349
CR1-CR11	SEMICOND,DIODE: SILICON	1N914	81349
IC1	INTEGRATED CKT: DUAL J-K CLOCKED FLIP-FLOP	SN158099N	01295
IC2	INTEGRATED CKT: DUAL 4-INPUT EXP. NAND GATE	SN15830N	01295
IC3	INTEGRATED CKT: HEX INVERTER	SN15836N	01295
IC4	SAME AS IC1		
IC5	INTEGRATED CKT: READ ONLY MEMORY	MM522	12040
IC6	INTEGRATED CKT: QUAD 2-INPUT NAND GATE	SN15846N	01295
7	SAME AS IC1		
IC8	SAME AS IC3		
IC9,IC10	INTEGRATED CKT: HEX INVERTER	SN7404N	01295

TABLE XIV (CONT'D)

REF DESIG	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
R1-R8	RES,FXD,COMP: 6.8K OHMS, ±5/5, 1/4W	RC07GF682J	81349
R9-R16	RES,FXD,COMP: 7.5K OHMS, ±5%, 1/4W	RC07GF752J	81349
R17,R18	RES,FXD,COMP: 10K OHMS, ±5%, 1/4W	RC07GF103J	81349
R19,R20	RES,FXD,COMP: 68 OHMS, ±5%, 1/2W	RC20GF680J	81349
VR1,VR2	SEMICOND,DIODE: ZENER 12V, 1W	1N4742	04713

TABLE XV

CIRCUIT CARD ASSEMBLY, CHARACTER DISTR & TIMING CONTROL: A7, 80372070-

REF DESIG	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
C1	CAP,FXD,CERAMIC: 2000PF, 1000V	DD202	71590
C2	CAP,FXD,MICA: 150PF, ±5%, 500V	DM15F151J0500 WV4CR	72136
C3	CAP,FXD,CERAMIC: 0.01UF, ±35%, 100V	TA01UF	91418
C4	CAP,FXD,ELCTLT: 4.7UF, ±20%, 10V	CS13BC475M	81349
CR1-CR3	SEMICOND,DIODE: GERMANIUM	1N277	81349
CR4	SEMICOND,DIODE: SILICON	1N914	81349
CR5,CR6	SAME AS CR1		
IC1,IC2	INTEGRATED CKT: QUAD 2-INPUT NAND GATE	SN15846N	01295
IC3	INTEGRATED CKT: HEX INVERTER	SN15836N	01295
IC4	INTEGRATED CKT: TRIPLE: 3-INPUT NAND/ NOR GATE	SN15862N	01295
IC5	INTEGRATED CKT: DUAL J-K CLOCKED FLIP-FLOP	SN15093N	01295
IC6	INTEGRATED CKT: DUAL 4-INPUT EXP. NAND GATE	SN15830N	01295
IC7,IC8	SAME AS IC3		
IC9,IC10	INTEGRATED CKT: 5 BIT SHIFT REGISTER	SN7496N	01295
Q1	TRANSISTOR: NPN	2N706	81349
Q2	TRANSISTOR: NPN	2N708	81349
R1-R3	RES,FXD,COMP: 10K OHMS, ±5%, 1/4W	RC07GF103J	81349
R4	RES,FXD,COMP: 62K OHMS, ±5%, 1/4W	RC07GF623J	81349
R5	RES,FXD,COMP: 39K OHMS, ±5%, 1/4W	RC07GF393J	81349

TABLE XV (CONT'D)

REF DESIG	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
R6	RES,FXD,COMP: 2K OHMS, ±5%, 1/4W	RC07GF202J	81349
R7	RES,FXD,COMP: 220 OHMS, ±5%, 1/4W	RC07GF221J	81349
R8	RES,FXD,COMP: 5.1K OHMS, ±5%, 1/4W	RC07GF512J	81349
R9	RES,FXD,COMP: 1.2K OHMS, ±5%, 1/4W	RC07GF122J	81349
R10	RES,FXD,COMP: 2.2K OHMS, ±5%, 1/4W	RC07GF222J	81349
R11	RES,FXD,COMP: 100K OHMS, ±5%, 1/4W	RC07GF104J	81349
R12	RES,FXD,COMP: 6.8K OHMS, ±5%, 1/4W	RC07GF682J	81349
R13,R14	NOT USED		
R15,R16	SAME AS R1		

TABLE XVI

CIRCUIT CARD ASSEMBLY, SIGNAL PATTERN MATRIX: A8, 80372080-000

REF DESIG	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
C1	CAP,FXD,ELCTLT: 4.7UF, ±20%, 10V	CS13BC475M	81349
C2	CAP,FXD,CERAMIC: 0.01UF, ±35%, 100V	TA01UF	91418
CR1-CR11	SEMICOND,DIODE: SILICON	1N914	81349
IC1	INTEGRATED CKT: DUAL 4-INPUT EXP. NAND GATE	SN15830N	01295
IC2	INTEGRATED CKT: HEX INVERTER	MC840P	04713
IC3,IC4	SAME AS IC1		
IC5-IC7	INTEGRATED CKT: QUAD 2-INPUT NAND GATE	SN15846N	01295
IC8	INTEGRATED CKT: HEX INVERTER	SN15836N	01295
IC9	INTEGRATED CKT: BCD-TO-DECIMAL 4-10 LINE DECODER	SN7442N	01295
IC10	SAME AS IC8		
IC11,IC12	SAME AS IC5		
R1-R3	RES,FXD,COMP: 10K OHMS, ±5%, 1/4W	RC07GF103J	81349

TABLE XVII

CIRCUIT CARD ASSEMBLY, EXTENDER CARD: A9, 80372180-000

REF DESIG	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
J1	CONN,RCPT,ELEC: 22 PIN, DUAL	225-22221-10500	02660

TABLE XVIII

CIRCUIT CARD ASSEMBLY, PATTERN GEN HARNESS CARD: A10 80372090-00

REF DESIG	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
XA1-XA10	CONN,RCPT,ELEC: 22 PIN	252-22-30-220	71785

TABLE XVIX

CRYSTAL BRACKET ASSEMBLY: A11 90372006-000

REF DESIG	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
R1-R7	RES,FXD,COMP: 1K OHMS, ±5% 1/4W	RC07GF102J	81349
SI	SWITCH,ROTARY:	C212-26036-2-1	71450
XY1-XY7	SOCKET,CRYSTAL:	TS0205P01	81349

TABLE XX

POWER SUPPLY, PATTERN GENERATOR: A12, 90372004-000

REF DESIG	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
C1	CAP,FXD,ELCTLT: 4600UF, 15V	36D462G015AA2A	56289
E1-E4	TERMINAL,STANDOFF:	4820-1-0516	71279
E5,E6	TERMINAL,STANDOFF	4821-1-0516	71279
F1	FUSE,CARTRIDGE: 1/4 AMP-3AG	312-250	75915
J1	CONN,RCPT,ELEC:	7595	74545
J2	CONN,RCPT,ELEC: COAXIAL	UG1094U	81349
R1	RES,FXD,WW: 3-3K, 5W	RW67V332	81349
SI	SWITCH,TOGGLE: SPDT	MST105D	95146
T1	TRANSFOMER,PWR: 47HZ, 132 VAC	43000276-000	96238
TB1,TB2	TERMINAL BOARD: 7 TERM	599-2004-7	75382
XF1	FUSEHOLDER:	HKP	71400

TABLE XXI

CIRCUIT CARD ASSEMBLY, SELECTOR SWITCH: A14, 80372200-000

REF DESIG	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
CR1-CR8	SEMICOND,DIODE: SILICON	1N914	81349
S10-S15	SWITCH,PB: SEQ CHAR	46027641-000	96238

TABLE XXII
PART NUMBER - NATIONAL STOCK NUMBER
CROSS REFERENCE INDEX

PART NUMBER	FSCM	NATIONAL STOCK NUMBER	PART NUMBER	FSCM	NATIONAL STOCK NUMBER
CS13BF105K	81349	5910-00-787-2109	RC07GF393J	81349	5905-00-115-8055
CS13BF156K	81349	5910-00-779-4968	RC07GF471J	81349	5905-00-120-9154
CS13BF226K	81349	5910-00-779-8390	RC07GF471J	81349	5905-00-683-2242
DD202	71590	5910-00-044-6034	RC07GF473J	81349	5905-00-683-2246
DD202	71590	5910-00-538-1508	RC07GF512J	81349	5905-00-683-2241
DM15F101J0500WV4CR	72136	5910-00-984-7588	RC07GF513J	81349	5905-00-682-4103
DM15F151J0500WV4CR	72136	5910-01-030-1770	RC07GF561J	81349	5905-00-682-4109
HKP	71400	5920-00-892-9311	RC07GF621J	81349	5905-00-801-6998
MC858P	04713	5962-00-184-8205	RC07GF622J	81349	5905-00-682-4100
MSP105F	95146	5930-00-059-3399	RC07GF623J	81349	5905-00-682-4104
MST105D	95146	5930-00-902-4150	RC07GF681J	81349	5905-00-727-8001
N112A	82389	5935-00-893-3935	RC07GF682J	81349	5905-00-110-7622
RC07GF101J	81349	5905-00-683-7721	RC07GF683J	81349	5905-00-119-3505
RC07GF102J	81349	5905-00-681-6462	RC07GF752J	81349	5905-00-682-4101
RC07GF103J	81349	5905-00-683-2238	RC07GF822J	81349	5905-00-831-6134
RC07GF104J	81349	5905-00-110-0388	RC20GF102J	81349	5905-00-110-0196
RC07GF104J	81349	5905-00-686-3129	RC20GF220J	81349	5905-00-279-3519
RC07GF122J	81349	5905-00-686-9994	RC20GF680J	81349	5905-00-116-8566
RC07GF152J	81349	5905-00-683-7723	RC20GF681J	81349	5905-00-111-8357
RC07GF153J	81349	5905-00-681-8818	RC20GF681J	81349	5905-00-111-8357
RC07GF181J	81349	5905-00-097-9534	RC42GF390J	81349	5905-00-279-3418
RC07GF183J	81349	5905-00-687-0000	RN55D1501F	81349	5905-00-728-1659
RC07GF202J	81349	5905-00-686-3370	RN55D4530F	81349	5905-00-913-5086
RC07GF203J	81349	5905-00-686-3368	RN55D6191F	81349	5905-00-965-9088
RC07GF221J	81349	5905-00-683-2240	RW67V1R0	81349	5905-00-081-7348
RC07GF222J	81349	5905-00-723-5251	RW67V332	81349	5905-00-975-1139
RC07GF223J	81349	5905-00-687-0002	SN158093N	01295	5962-00-103-4463
RC07GF242J	81349	5905-00-683-7724	SN158093N	01295	5962-00-103-4463
RC07GF302J	81349	5905-00-682-4097	SN158094N	01295	5962-00-163-4166
RC07GF332J	81349	5905-00-681-9969	SN158099N	01295	5962-00-420-6545
RC07GF333J	81349	5905-00-686-3903	SN15830N	01295	5962-00-011-2962
RC07GF362J	81349	5905-00-805-9714	SN15836N	01295	5962-00-193-0323

TABLE XXII
PART NUMBER - NATIONAL STOCK NUMBER
CROSS REFERENCE INDEX (CONT'D)

PART NUMBER	FSCM	NATIONAL STOCK NUMBER	PART NUMBER	FSCM	NATIONAL STOCK NUMBER
SN15845N	01295	5962-00-011-3010	46020383-000	96238	5930-01-009-7615
SN15846N	01295	5962-00-819-2215	46020386-000	96238	5930-01-013-8409
SN15849N	01295	5962-00-130-0353	46020388-000	96238	5930-01-013-8410
SN15862N	01295	5962-00-927-1749	46020389-000	96238	5930-01-013-8411
SN7404N	01295	5962-00-404-2559	46020391-000	96238	5930-01-013-7293
SN7442N	01295	5962-00-193-0329	46020397-000	96238	5930-01-013-7294
SN7490N	01295	5962-00-102-7519	46027640-000	96238	5930-01-010-7648
SN7493N	01295	5962-00-102-7520	46027641-000	96238	5930-01-010-7649
SN7496N	01295	5962-00-404-6174	4821-1-0516	71279	5940-00-901-4899
TGS50	56289	5910-00-577-3281	5GAD10	56289	5910-00-822-5682
TSO205P01	81349	5935-00-581-6941	5GAD10	56289	5910-00-822-5682
1N1614	81349	5961-00-410-3858	507-3905-1437-500	72619	6240-00-001-1524
1N4742	04713	5961-00-076-1403	599-2004-7	75382	5940-00-229-6900
1N645	81349	5961-00-577-6084	74000000-002	96238	5995-01-010-0022
1N746	81349	5961-00-847-5246	7571	74545	5935-00-480-7278
1N914	81349	5961-00-022-5664	7595	74545	5935-00-937-4219
111-102	74970	5940-00-615-2282	80372010-000	96238	6625-00-205-0294
111-103	74970	5940-00-688-2770	80372020-000	96238	6625-00-205-0298
2N2646	04713	5961-00-902-1177	80372030-000	96238	6625-00-205-0299
200P1-201	80294	5905-00-801-6213	80372040-000	96238	6625-00-207-9851
200P1-501	80294	5905-00-682-4142	80372050-000	96238	6625-00-207-9922
312-125	75915	5920-00-082-7437	80372060-000	96238	6625-00-213-2624
312-250	75915	5920-00-280-4181	80372070-000	96238	6625-00-207-9930
312-750	75915	5920-00-881-6775	80372080-000	96238	6625-00-213-2620
36D462G015AA2A	56289	5910-00-828-7905	80372090-000	96239	6625-00-213-2621
39D257G030EL4	56289	5910-00-927-5130	80372180-000	96238	6625-00-213-2686
40001213-000	96238	5961-00-584-2365	80372200-000	96238	6625-00-209-5333
40040082-004	96238	5955-01-009-4538	90372005-000	96238	5935-01-009-5653
40040082-005	96238	5955-01-009-4539			

APPENDIX A

REFERENCES

DA Pam 310-4	Index of Technical Publications: Technical Manuals, Technical Bulletins, Supply Manuals (Types 7, 8, and 9), Supply Bulletins, and Lubrication Orders.
DA Pam 310-7	US Army Equipment Index of Modification Work Orders.
TM 38-750	The Army Maintenance Management System (TAMMS).
TM 750-244-2	Procedures for Destruction of Electronics Materiel to Prevent Enemy Use. (Electronics Command).

APPENDIX B

COMPONENTS OF END ITEM LIST

Section I. INTRODUCTION

B-1. Scope

This appendix lists integral components of and basis issue items for the Signal Generator SG-1054/G to help you inventory items required for safe and efficient operation.

B-2. General

This Components of End Item List is divided into the following sections:

a. Section II. Integral Components of the End Item. These items, when assembled, comprise the Signal Generator SG-1054/G and must accompany it whenever it is transferred or turned in. The illustrations will help you identify these items.

b. Section III. Basic Issue Items. These are the minimum essential items required to place the Signal Generator SG–1054/G in operation, to operate it, and to perform emergency repairs. Although shipped separately packed, they must accompany the SG-1054/G during operation and whenever it is transferred between accountable officers. The illustrations will assist you with hard-to-identify items. This manual is your authority to requisition replacement BII, based on TOE/MTOE authorization of the end item.

B-3. Explanation of Columns

a. Illustration. This column is divided as follows:

(1) Figure number. Indicates the figure number of the illustration on which the item is shown.

(2) Item number. Not applicable.

b. National Stock Number. Indicates the National stock number assigned to the item and which will be used for requisitioning.

c. Description. Indicates the Federal item name and, if required, a minimum description to identify the item. The part number indicates the primary number used by the manufacturer, which controls the design and characteristics of the item by means of its engineering drawings, specifications, standards, and inspection requirements to identify an item or range of items. Following the part number, the Federal Supply Code for Manufacturers (FSCM) is shown in parentheses.

d. Location. Not applicable.

e. Usable on Code. Not applicable.

f. Quantity Required (Qty Reqd). This column lists the quantity of each item required for a complete major item.

g. Quantity. This column is left blank for use during an inventory. Under the Rcvd column, list the quantity you actually receive on your major item. The Date columns are for your use when you inventory the major item.

SECTION II INTEGRAL COMPONENTS OF END ITEM

(1) ILLUSTRATION (A) FIG NO.	(B) ITEM NO.	(2) NATIONAL STOCK NUMBER	(3) DESCRIPTION		(4) LOCATION	(5) USABLE ON CODE	(6) QTY REQD	(7) QUANTITY RCVD	DATE
			PART NUMBER	(FSCM)					
1		6625-00-137-7738	SIGNAL GENERATOR SG-1054/G	(96238)			1		
			LINE CORD ASSEMBLY 74000054-000	(96238)			1		

SECTION III BASIC ISSUE ITEMS

(1) ILLUSTRATION (A) FIG NO.	(B) ITEM NO.	(2) NATIONAL STOCK NUMBER	(3) DESCRIPTION	(4) LOCATION	(5) USABLE ON CODE	(6) QTY REQD	(7) QUANTITY RCVD	DATE
			PART NUMBER (FSCM)					
			TECHNICAL MANUAL			1		
			TM 11-6625-2921-14&P					

APPENDIX D

MAINTENANCE ALLOCATION

Section I. INTRODUCTION

D-1. General

This appendix provides a summary of the maintenance operations for Signal Generator SG1054/G. It authorizes categories of maintenance for specific maintenance functions on repairable items and components and the tools and equipment required to perform each function. This appendix may be used as an aid in planning maintenance operations.

D-2 . Maintenance Function

Maintenance functions will be limited to and defined as follows:

a. Inspect. To determine the serviceability of an item by comparing its—physical, mechanical, and/or electrical characteristics with established standards through examination.

b . Test. To verify serviceability and to detect incipient failure by measuring the mechanical or electrical characteristics of an item and comparing those characteristics with prescribed standards.

c. Service. Operations required periodically to keep an item in proPer operating condition, i.e., to clean (decontaminate), to preserve, to drain, to paint, or to replenish fuel, lubricants, hydraulic fluids, or compressed air supplies.

d. Adjust. To maintain, within prescribed limits, by bringing into proper or exact position, or by setting the operating characteristics to the specified parameters.

e. Align. To adjust specified variable elements of an item to bring about optimum or desired performance.

f. Calibrate. To determine and cause corrections to be made or to be adjusted on instruments or test measuring and diagnostic equipments used in precision measurement. Consists of comparisons of two instruments, one of which is a certified standard of known accuracy, to detect and adjust any discrepancy in the accuracy of the instrument being compared.

g. Install. The act of emplacing, seating, or fixing into position an item, part, module (component or assembly) in a manner to allow the proper functioning of the equipment or system.

h. Replace. The act of substituting a serviceable like type part, subassembly, or module (component or assembly) for an unserviceable counterpart.

i. Repair. The application of maintenance services (inspect, test, service, adjust, align, calibrate, replace) or other maintenance actions (welding, grinding, riveting, straightening, facing, remachining, or resurfacing) to restore serviceability to an item by correcting specific damage, fault, malfunction, or failure in a part, subassembly, module (component or assembly), end item, or system.

j. Overhaul. That maintenance effort (service/action) necessary to restore an item to a completely serviceable/operational condition as prescribed by maintenance standards (i.e., DMWR) in appropriate technical publications. Overhaul is normally the highest degree of maintenance performed by the Army. Overhaul does not normally return an item to like new condition.

k. Rebuild. Consists of those services/actions necessary for the restoration of unserviceable equipment to a like new condition in accordance with original manufacturing standards. Rebuild is the highest degree of materiel maintenance applied to Army equipment. The rebuild operation includes the act of returning to zero those age measurements (hours, miles, etc.) considered in classifying Army equipments/components.

D-3. Column Entries

a. Column 1, Group Number. Column 1 lists group numbers, the purpose of which is to identify components, assemblies, subassemblies, and modules with the next higher assembly.

b. Column 2, Component/Assembly. Column 2 contains the noun names of components, assemblies, subassemblies, and modules for which maintenance is authorized.

c. Column 3, Maintenance Functions. Column 3 lists the functions to be performed on the item listed in column 2. When items are listed without maintenance functions, it is solely for purpose of having the group numbers in the MAC and RPSTL coincide.

d. Column 4, Maintenance Category. Column 4 specified, by the listing of a "work time" figure in the appropriate subcolumn(s), the lowest level of maintenance authorized to perform the function listed in column 3. This figure represents the active time required to perform that maintenance function at the indicated category of maintenance. If the number or complexity of the tasks within the listed maintenance function vary at different maintenance categories, appropriate "work time" figures will be shown for each category. The number of task-hours specified by the "work time" figure represents the average time required to restore an item (assembly, subassembly, component, module, end item

or system) to a serviceable condition under typical field operating conditions. This time includes preparation time, troubleshooting time, and quality assurance/quality control time in addition to the time required to perform the specific tasks identified for the maintenance functions authorized in the maintenance allocation chart. Subcolumns of column 4 are as follows:

C - Operator/Crew

O - Organizational

F - Direct Support

H - General Support

D - Depot

e. Column 5, Tools and Equipment. Column 5 specifies by code, those tom—on tool sets (not individual tools) and special tools, test, and support equipment required to perform the designated function.

f. Column 6, Remarks. Column 6 contains an alphabetic code which leads to the remark in section IV, Remarks, which is pertinent to the item opposite the particular code.

D-4. Tool and Test Equipment Requirements (Section III)

a. Tool or Test Equipment Reference Code. The numbers in this column coincide with the numbers used in the tools and equipment column of the MAC. The numbers indicate the applicable tool or test equipment for the maintenance functions.

b. Maintenance Category. The codes in this column indicate the maintenance category allocated the tool or test equipment.

c. Nomenclature. This column lists the noun name and nomenclature of the tools and test equipment required to perform the maintenance functions.

d. National/NATO Stock Number. This column lists the National/NATO stock number of the specific tool or test equipment.

e. Tool Number. This column lists the manufacturer's part number of the tool followed by the Federal Supply Code for Manufacturers (5-digit) in parentheses.

D-5. Remarks (Section IV

a. Reference Code. This code refers to the appropriate item in section II, column 6.

b. Remarks. This column provides the required explanatory information necessary to clarify items appearing in section II.

SECTION II MAINTENANCE ALLOCATION CHART

FOR

GENERATOR, SIGNAL SG-1054/G

(1) GROUP NUMBER	(2) COMPONENT/ASSEMBLY	(3) MAINTENANCE FUNCTION	(4) MAINTENANCE CATEGORY					(5) TOOLS AND EQPT.	(6) REMARKS
			C	O	F	H	D		
00	GENERATOR, SIGNAL SG-1054/G	Inspect[1]	0.2					7	
		Test[2]	0.3						
		Test				0.5		1 thru 5	
		Service	0.4					7	
		Repair	0.2					7	
		Repair				0.5		6	
		Overhaul					3.0	1 thru 6	
01	CIRCUIT CARD ASSEMBLY 80372010 TIME BASE LOGIC (A1)	Test[3]				0.5		1 thru 5	
		Repair				0.6		6	
0101	CIRCUIT CARD ASSEMBLY OSCILLATOR (A1A1)	Test[3]				0.3		1 thru 5	
		Repair				0.5		6	
02	CIRCUIT CARD ASSEMBLY 80372020 (A2)	Test[3]				0.5		1 thru 5	
		Repair						6	
03	CIRCUIT CARD ASSEMBLY 80372030 (A3)	Test[3]				0.5		1 thru 5	
		Repair				0.6		6	
04	CIRCUIT CARD ASSEMBLY 80372040 (A4)	Test[3]				0.5		1 thru 5	
		Repair				0.6		6	
05	CIRCUIT CARD ASSEMBLY 80372050 (A5)	Test[3]				0.5		1 thru 5	
		Repair				0.6		6	
06	CIRCUIT CARD ASSEMBLY 80372060 (A6)	Test[3]				0.5		1 thru 5	
		Repair				0.6		6	
07	CIRCUIT CARD ASSEMBLY 80372070 (A7)	Test[3]				0.5		1 thru 5	
		Repair				0.6		6	
08	CIRCUIT CARD ASSEMBLY 80372080 (A8)	Test[3]				0.5		1 thru 5	
		Repair				0.6		6	
09	CIRCUIT CARD ASSEMBLY 80372180 (A9)	Test[3]				0.5		1 thru 5	
		Repair				0.6		6	
10	CIRCUIT CARD ASSEMBLY 80372090 (A10)	Test[3]				0.5		1 thru 5	
		Repair				0.6		6	
11	CRYSTAL BRACKET ASSEMBLY 90372006 (A11)	Test						1 thru 5	
		Repair						6	
12	POWER SUPPLY, PATTERN GENERATOR 90372004 (A12)	Test						1 thru 5	
		Repair						6	
13	CIRCUIT CARD ASSEMBLY 80372200 (A14)	Test						1 thru 5	
		Repair						6	

NOTES: [1] Visual only.
[2] Simple Operational Checks
[3] Test as part of end item

SECTION III TOOL AND TEST EQUIPMENT REQUIREMENTS
FOR
GENERATOR, SIGNAL SG-1054/G

TOOL OR TEST EQUIPMENT REF COD	MAINTEN CATEGORY	NOMENCLATURE	NATIONAL/NATO STOCK NUMBER	TOOL NUMBER
1	H,D	ANALYZER, DATA, TELE	PENDING	
2	H,D	COUNTER, ELECTRONIC,	6625-00-044-3228	
3	H,D	MULTIMETER, AN/USM-2	6625-00-999-7465	
4	H,D	OSCILLOSCOPE, AN/USM	6625-00-106-9622	
5	H,D	TELETYPEWRITER, TT-4	PENDING	
6	H,D	TOOL KIT, TK-100/G	5180-00-605-0079	

TOOLS AND TEST EQUIPMENT AVAILABLE TO THE OPERATOR BECAUSE OF HIS/HER ASSIGNED MISSION.

APPENDIX F

REPAIR PARTS AND SPECIAL TOOLS LIST

Refer to Section 5, Parts List, for all maintenance parts.

By Order of the Secretary of the Army:

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General, United States Army
Chief of Staff

Official:

J. C. PENNINGTON
Major General, United States Army
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Ft Carson (5)
Ft Gillem (5)
Ft Richardson (CERCOM Ofc) (2)
WSMR (1)
USAERDAA (1)
USAERDAW (1)
Army Dep (1) except
LBAD (10)
SHAD (3)
SAAD (30)
TOAD (14)
USA Dep (1)
Sig Sec USA Dep (1)
Units Org Under Fol TOE:
29-134 (1)
29-136 (1)
29-207 (1)
29-610 (1)

NG: None

USAR: None

For explanation of abbreviations used, see AR 310-50.

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DATE 10 July 1975

PUBLICATION NUMBER	DATE	TITLE
TM 11-5840-340-12	23 Jan 74	Radar Set AN/MPQ-76

BE EXACT. . .PIN-POINT WHERE IT IS

PAGE NO.	PARAGRAPH	FIGURE NO.	TABLE NO.	IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:
2-25	2-28			Recommend that the installation antenna alignment procedure be changed throughout to specify a 2° IFF antenna lag rather than 1°. REASON: Experience has shown that with only a 1° lag, the antenna servo system is too sensitive to wind gusting in excess of 20 knots, and has a tendency to rapidly accelerate and decelerate as it hunts, causing strain to the drive train. Hunting is minimized by adjusting the lag to 2° without degradation of operation.
3-10	3-3		3-1	Item 5, Function column. Change "2 db" to "3db." REASON: The adjustment procedure for the TRANS POWER FAULT indicator calls for a 3 db (500 watts) adjustment to light the TRANS POWER FAULT indicator.
5-6	5-8			Add new step f.1 to read, "Replace cover plate removed in step e.1, above." REASON: To replace the cover plate.
		F03		Zone C 3. On J1-2, change "+24 VDC to "+5 VDC." REASON: This is the output line of the 5 VDC power supply. + 24 VDC is the input voltage.

TYPED NAME, GRADE OR TITLE, AND TELEPHONE NUMBER
SSG I. M. DeSpiritof 999-1776

SIGN HERE: SSG I. M. DeSpiritof

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THE METRIC SYSTEM AND EQUIVALENTS

'NEAR MEASURE

. Centimeter = 10 Millimeters = 0.01 Meters = 0.3937 Inches
1 Meter = 100 Centimeters = 1000 Millimeters = 39.37 Inches
1 Kilometer = 1000 Meters = 0.621 Miles

'VEIGHTS

Gram = 0.001 Kilograms = 1000 Milligrams = 0.035 Ounces
1 Kilogram = 1000 Grams = 2.2 lb.
1 Metric Ton = 1000 Kilograms = 1 Megagram = 1.1 Short Tons

LIQUID MEASURE

1 Milliliter = 0.001 Liters = 0.0338 Fluid Ounces
1 Liter = 1000 Milliliters = 33.82 Fluid Ounces

SQUARE MEASURE

1 Sq. Centimeter = 100 Sq. Millimeters = 0.155 Sq. Inches
1 Sq. Meter = 10,000 Sq. Centimeters = 10.76 Sq. Feet
1 Sq. Kilometer = 1,000,000 Sq. Meters = 0.386 Sq. Miles

CUBIC MEASURE

1 Cu. Centimeter = 1000 Cu. Millimeters = 0.06 Cu. Inches
1 Cu. Meter = 1,000,000 Cu. Centimeters = 35.31 Cu. Feet

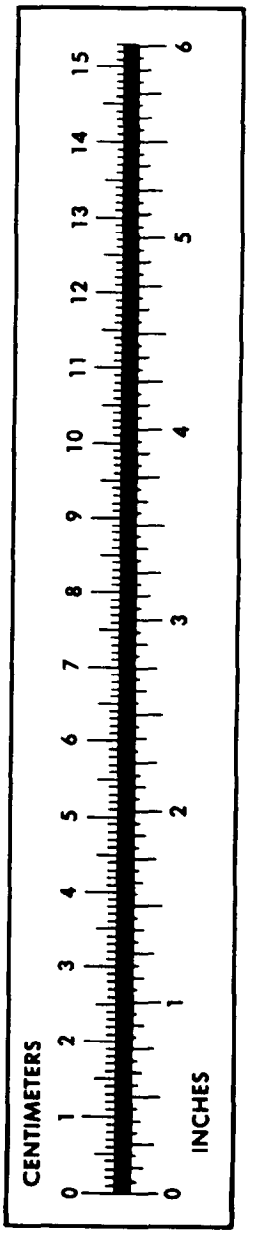
TEMPERATURE

5/9(°F - 32) = °C
212° Fahrenheit is evuivalent to 100° Celsius
90° Fahrenheit is equivalent to 32.2° Celsius
32° Fahrenheit is equivalent to 0° Celsius
9/5C° + 32 =°F

APPROXIMATE CONVERSION FACTORS

TO CHANGE	TO	MULTIPLY BY
Inches	Centimeters	2.540
Feet	Meters	0.305
Yards	Meters	0.914
Miles	Kilometers	1.609
Square Inches	Square Centimeters	6.451
Square Feet	Square Meters	0.093
Square Yards	Square Meters	0.836
Square Miles	Square Kilometers	2.590
Acres	Square Hectometers	0.405
Cubic Feet	Cubic Meters	0.028
Cubic Yards	Cubic Meters	0.765
Fluid Ounces	Milliliters	29.573
ıts	Liters	0.473
arts	Liters	0.946
allons	Liters	3.785
Ounces	Grams	28.349
Pounds	Kilograms	0.454
Short Tons	Metric Tons	0.907
Pound-Feet	Newton-Meters	1.356
Pounds per Square Inch	Kilopascals	6.895
Miles per Gallon	Kilometers per Liter	0.425
Miles per Hour	Kilometers per Hour	1.609

TO CHANGE	TO	MULTIPLY BY
Centimeters	Inches	0.394
Meters	Feet	3.280
Meters	Yards	1.094
Kilometers	Miles	0.621
Square Centimeters	Square Inches	0.155
Square Meters	Square Feet	10.764
Square Meters	Square Yards	1.196
Square Kilometers	Square Miles	0.386
Square Hectometers	Acres	2.471
Cubic Meters	Cubic Feet	35.315
Cubic Meters	Cubic Yards	1.308
Milliliters	Fluid Ounces	0.034
Liters	Pints	2.113
Liters	Quarts	1.057
ers	Gallons	0.264
ms	Ounces	0.035
ograms	Pounds	2.205
Metric Tons	Short Tons	1.102
Newton-Meters	Pounds-Feet	0.738
Kilopascals	Pounds per Square Inch	0.145
lometers per Liter	Miles per Gallon	2.354
meters per Hour	Miles per Hour	0.621



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